VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches

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Motivation

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- **Contribution: VARIUS-TC**

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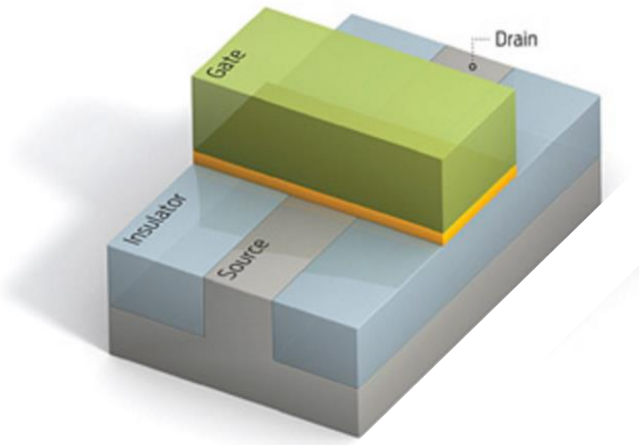
- **Contribution: VARIUS-TC**
  - Modeling process variation in **emerging devices** at **architecture-level**.

Thin Channel (TC) devices

[K. Ahmed, and K. Schuegraf. "Transistor wars." *IEEE Spectrum*48.11 (2011): 50-66.].

Thin Channel (TC) devices

Traditional Planar CMOS



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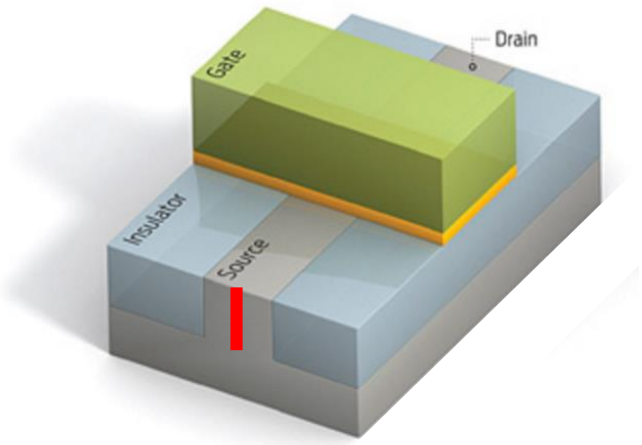

Channel Thickness

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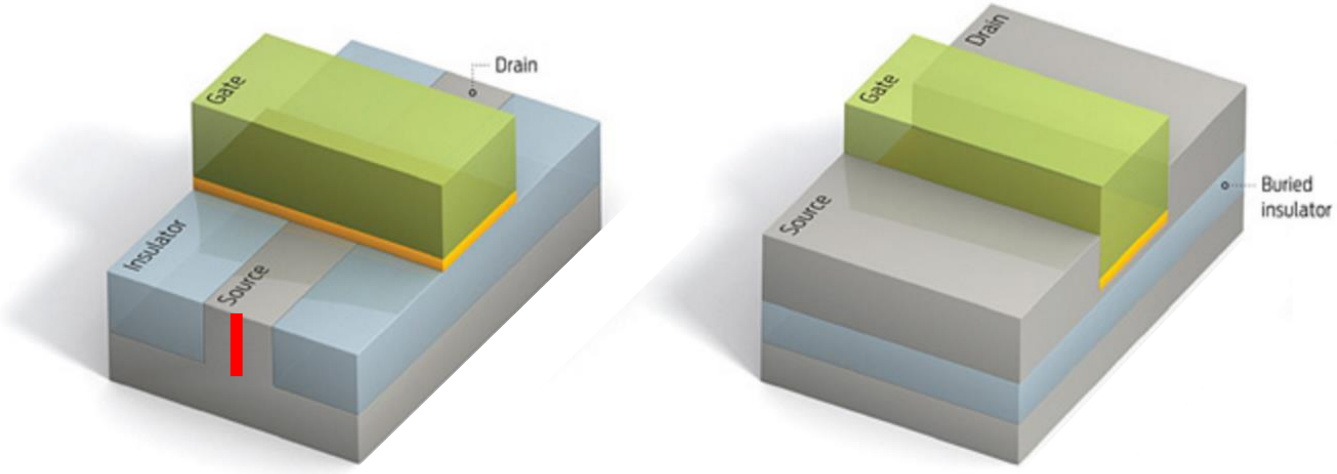

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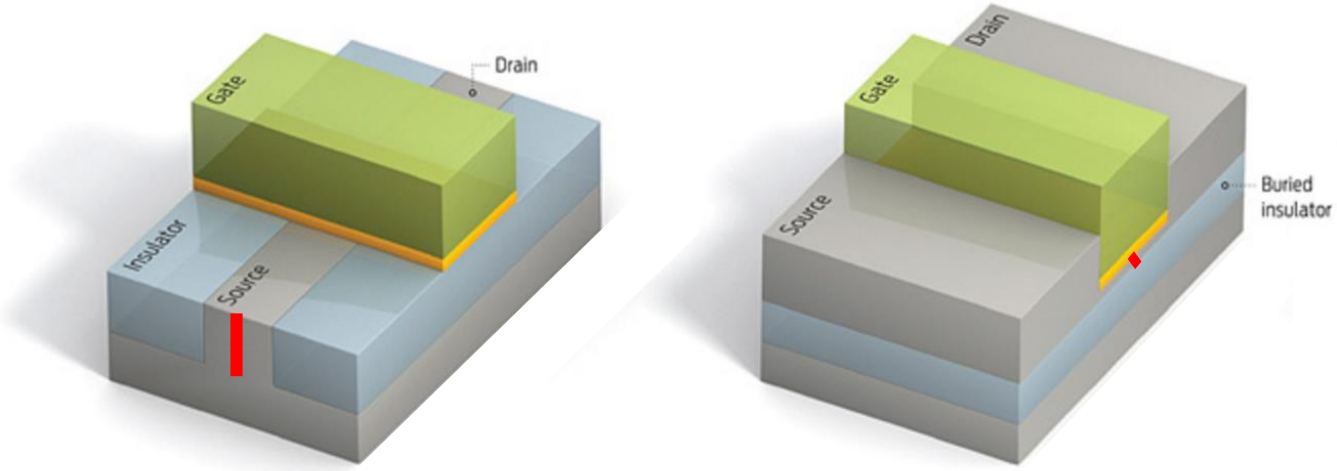

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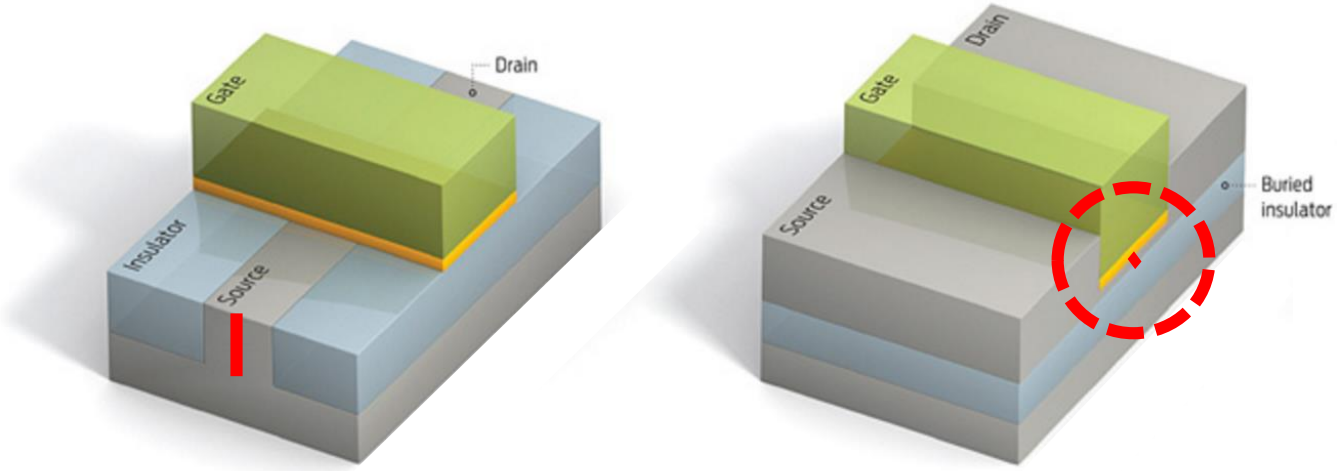

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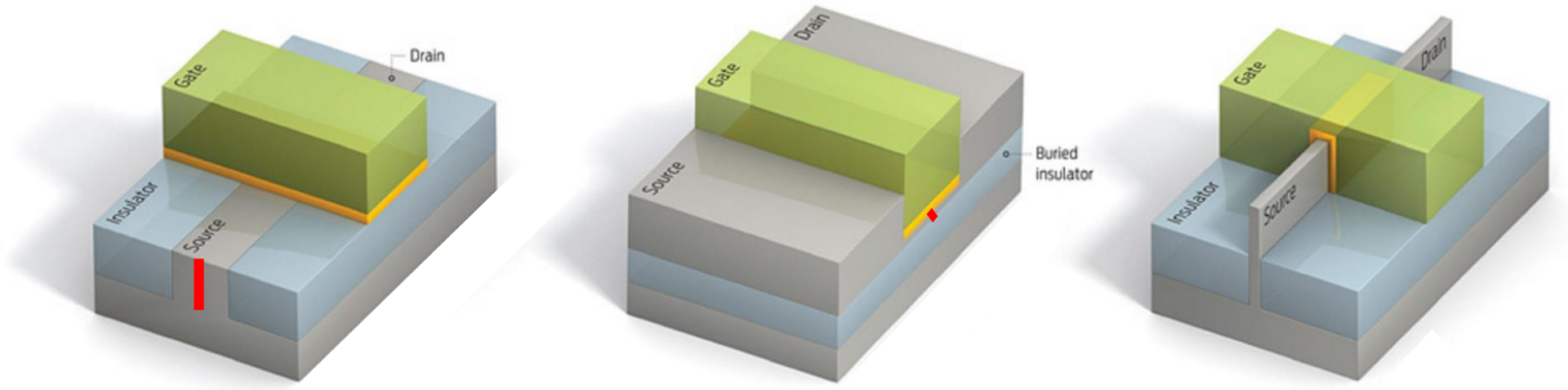

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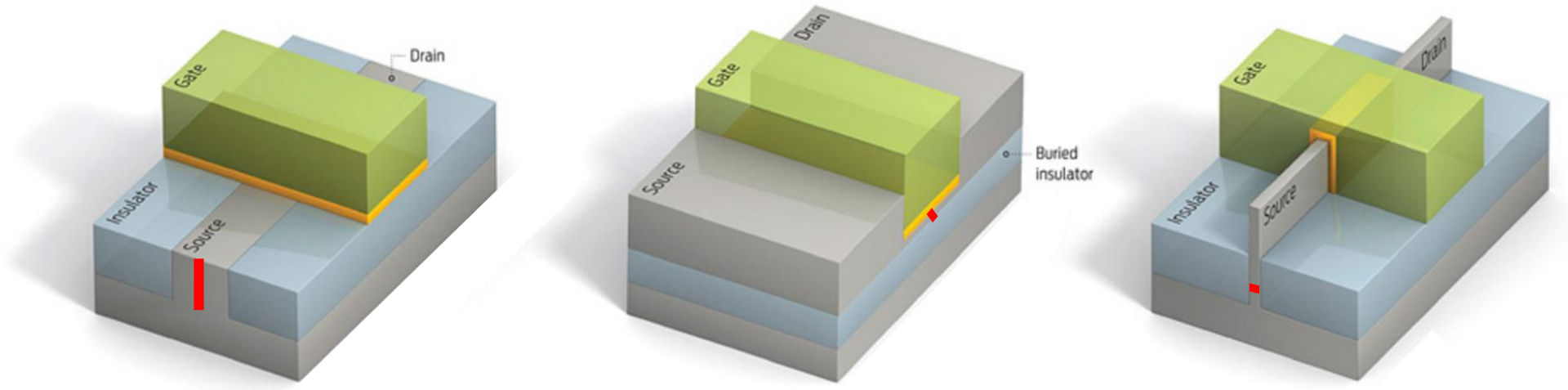

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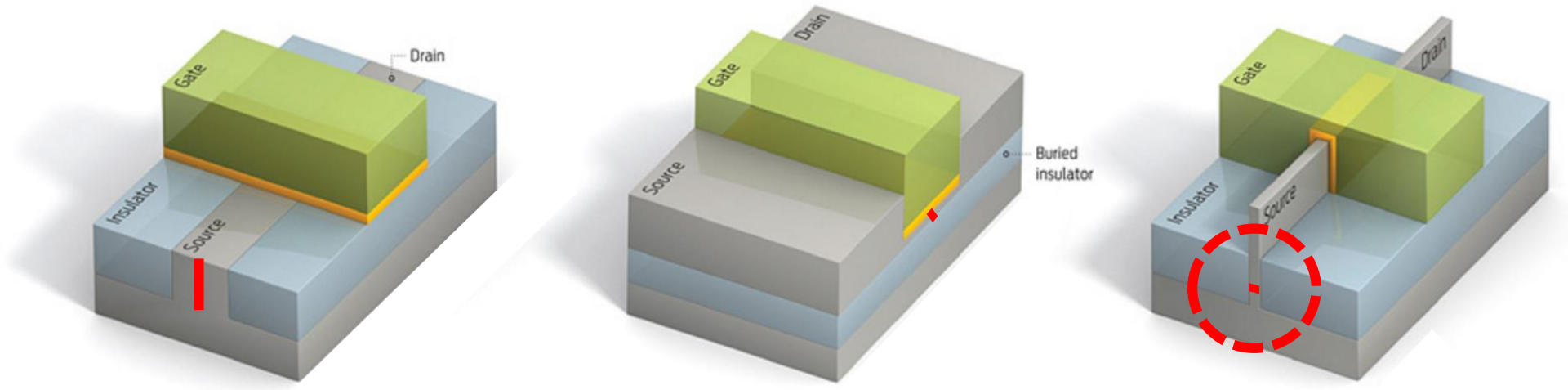

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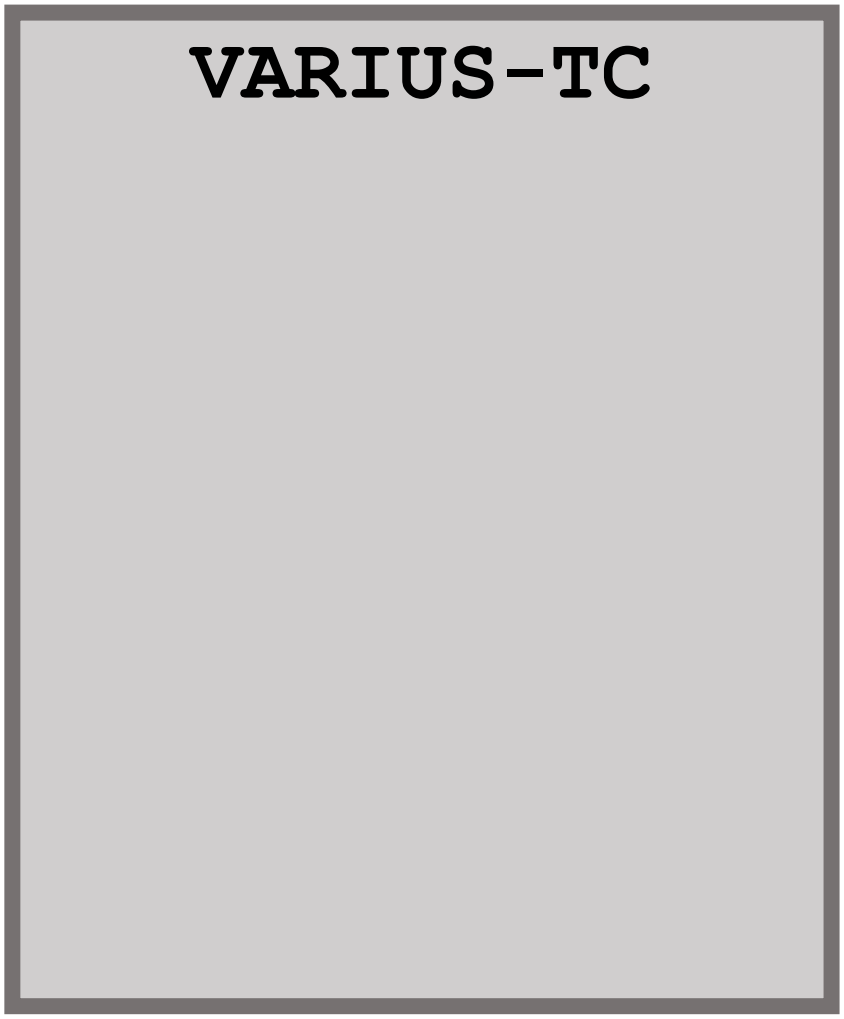

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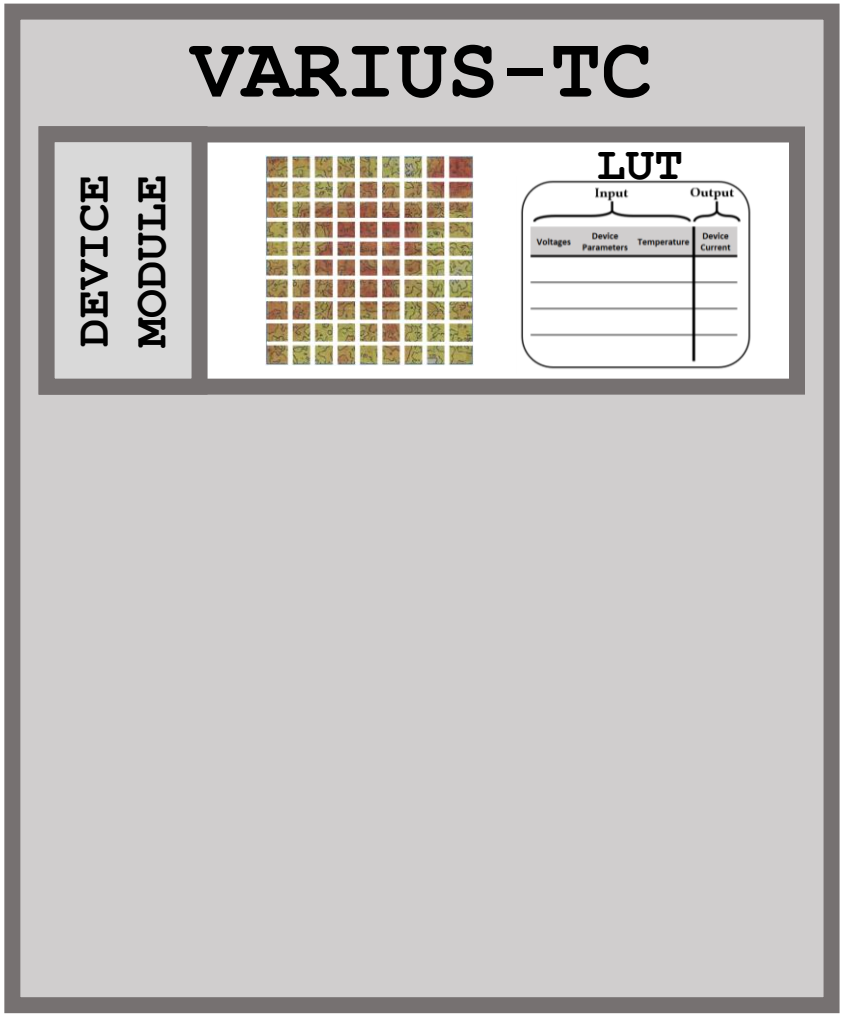

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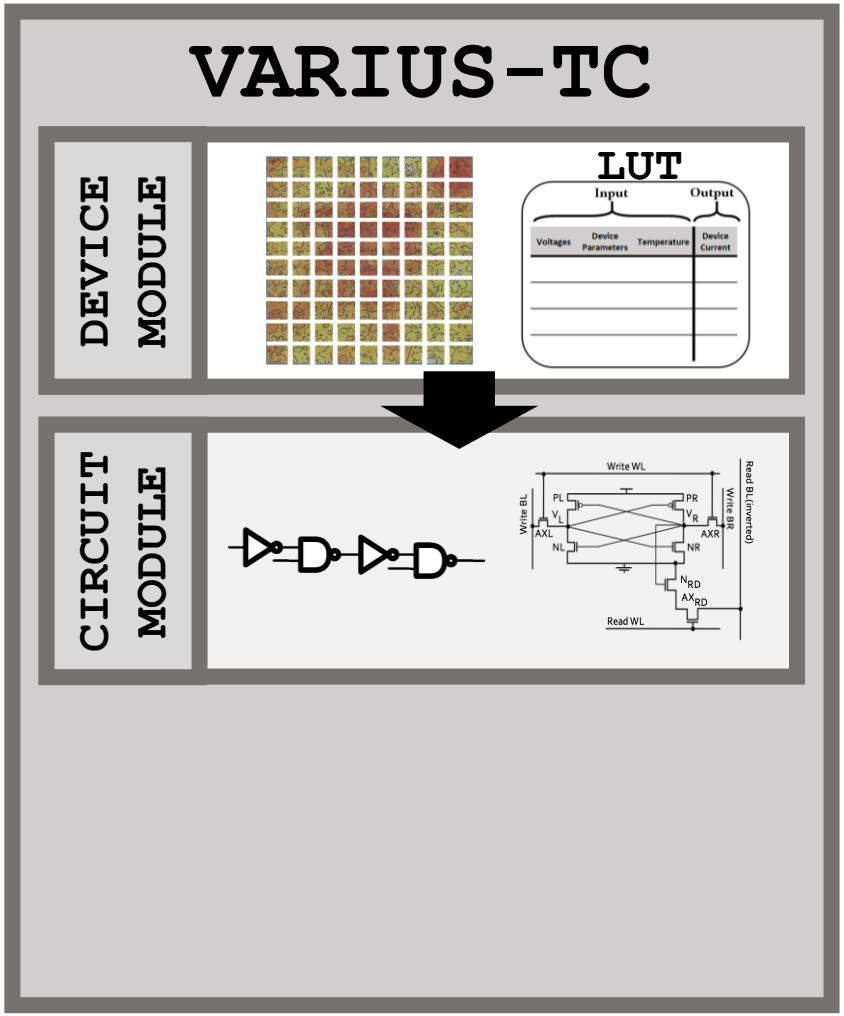

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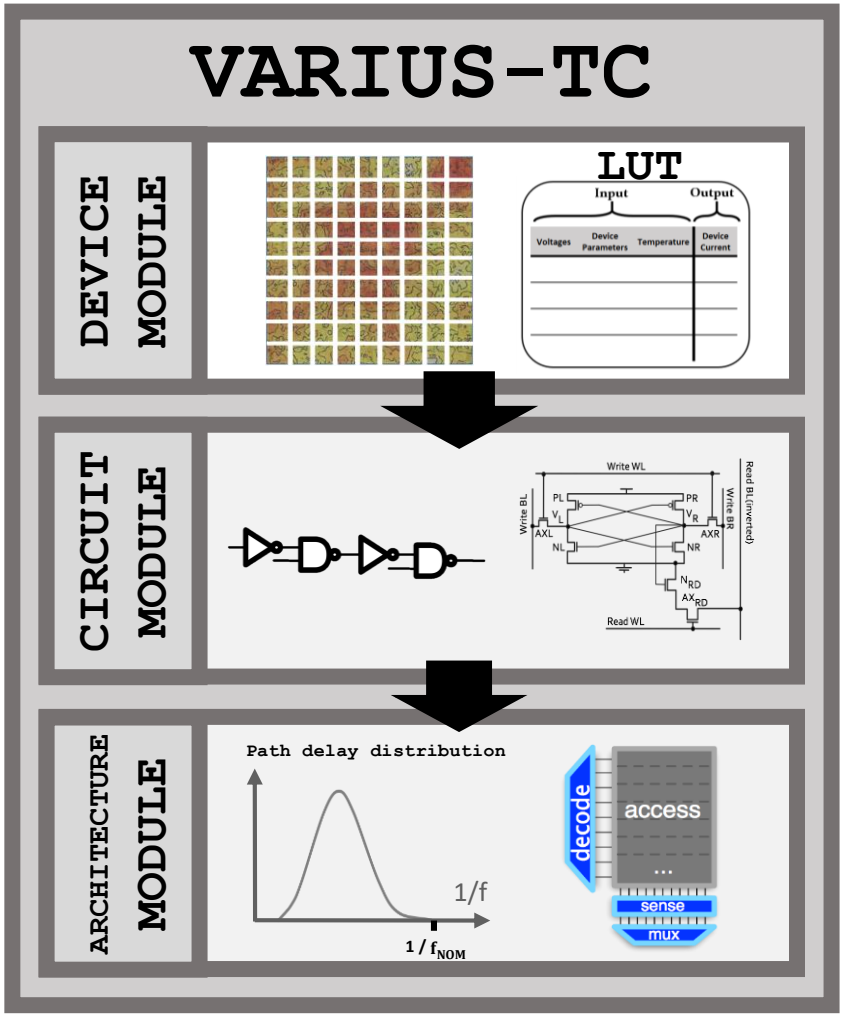

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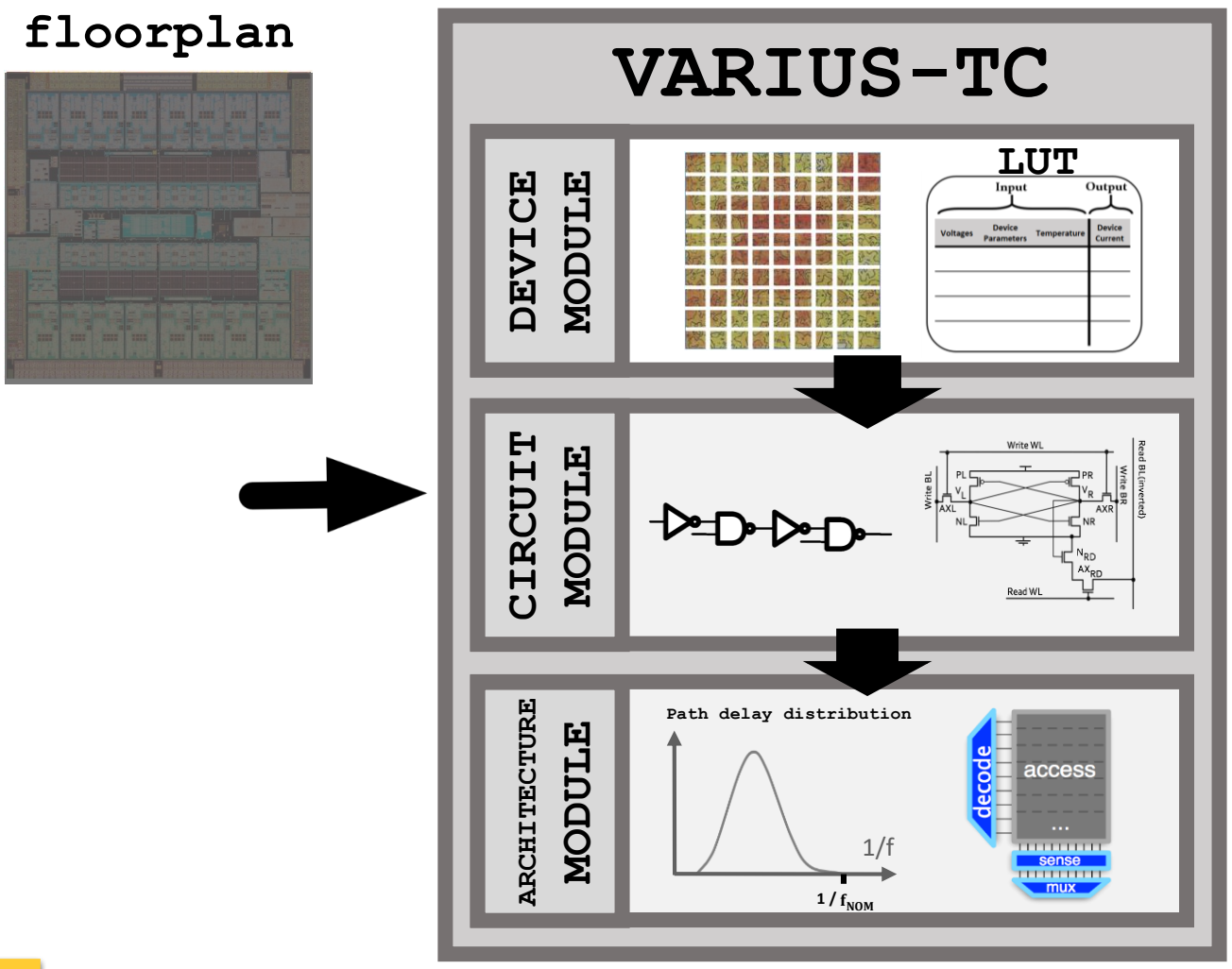
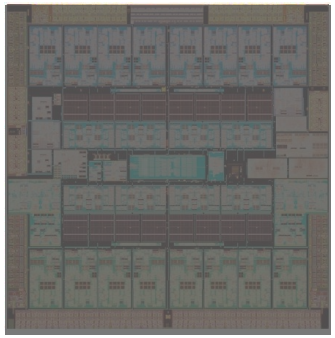
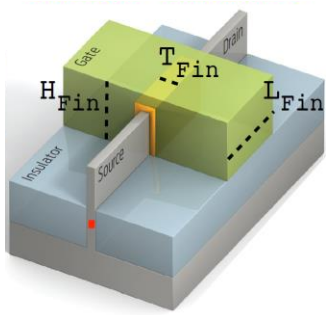


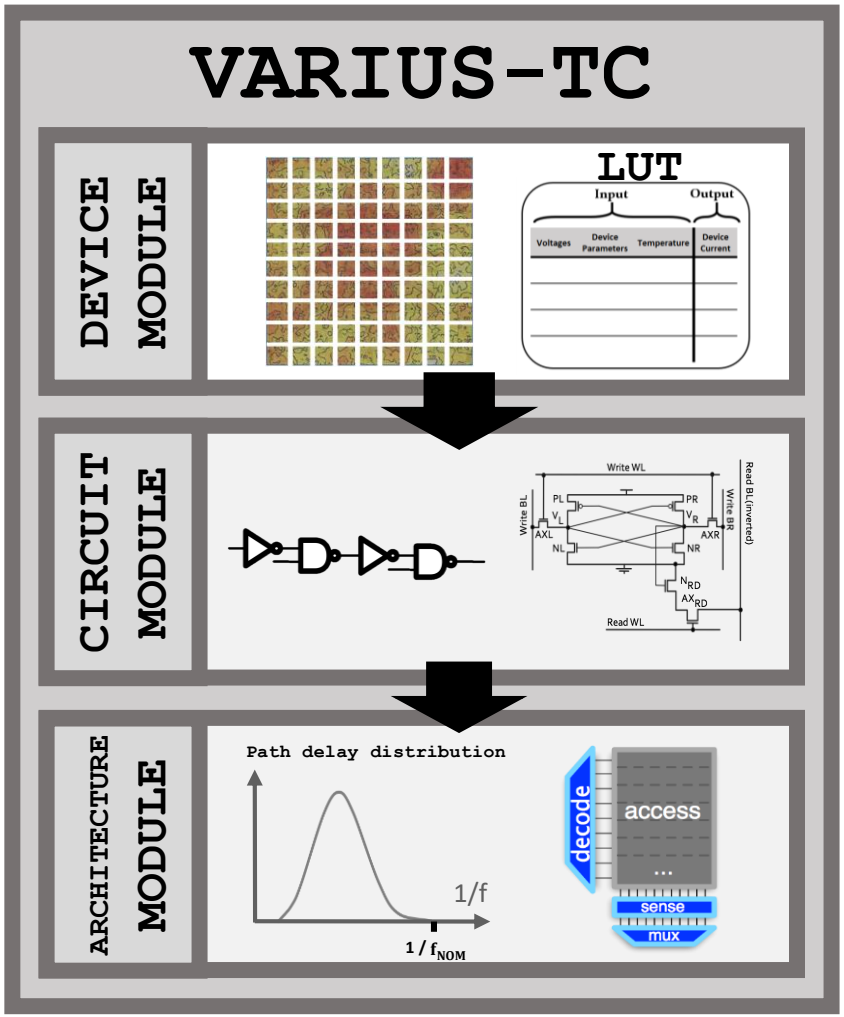
VARIUS-TC: Overview

floorplan



device parameters





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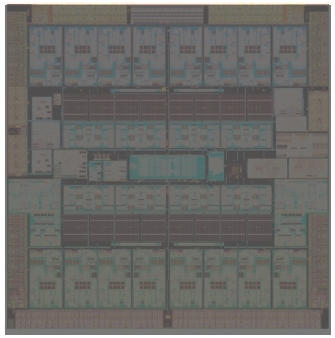

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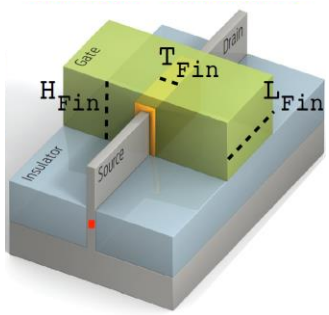
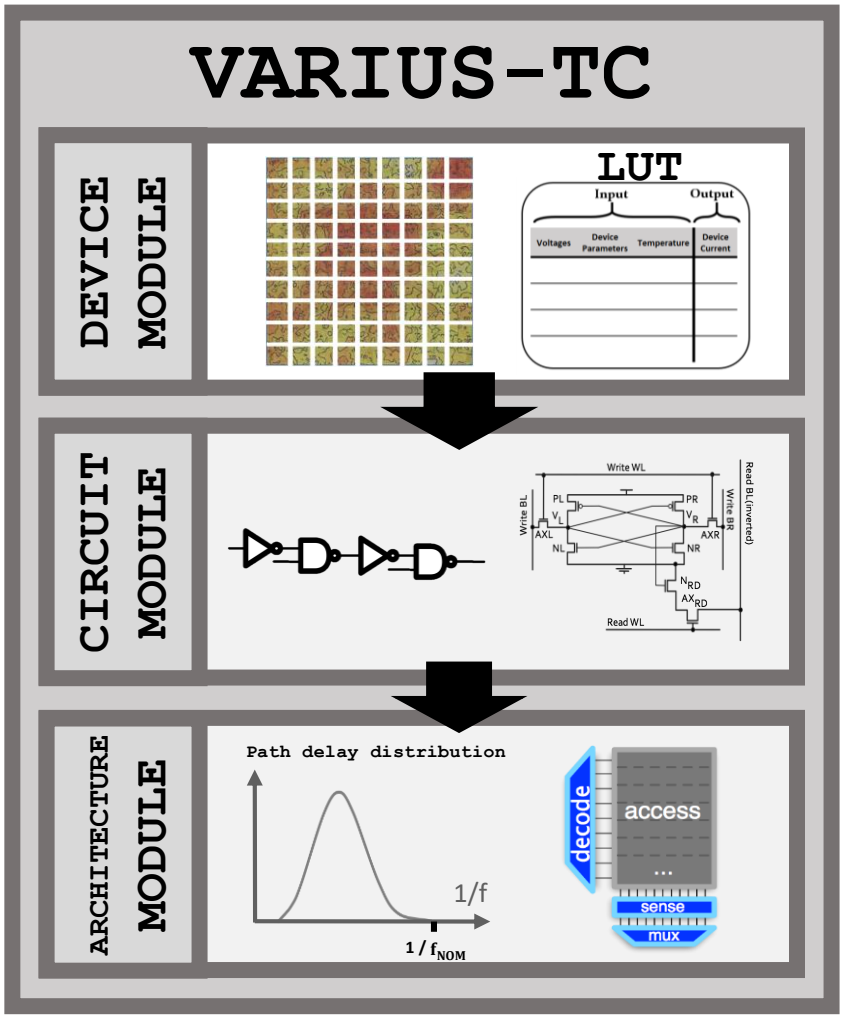
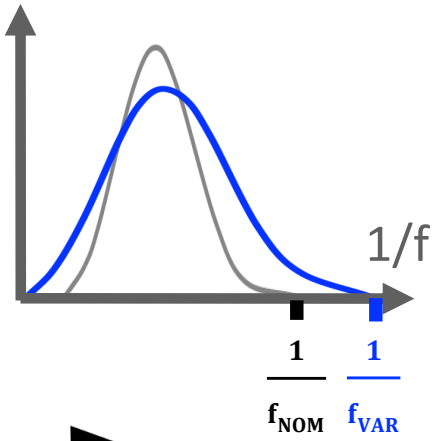




Path delay distribution



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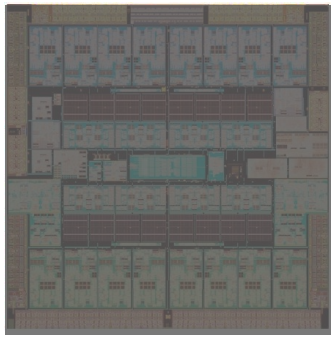

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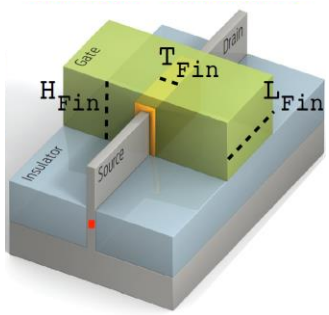

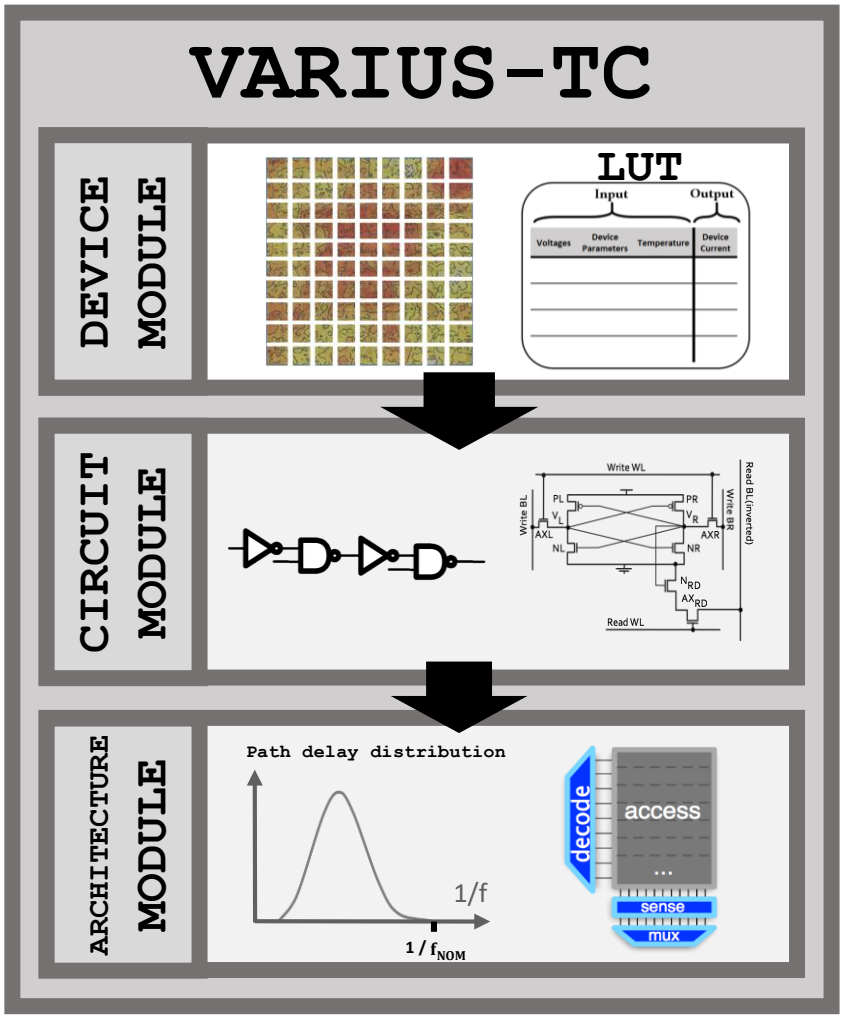

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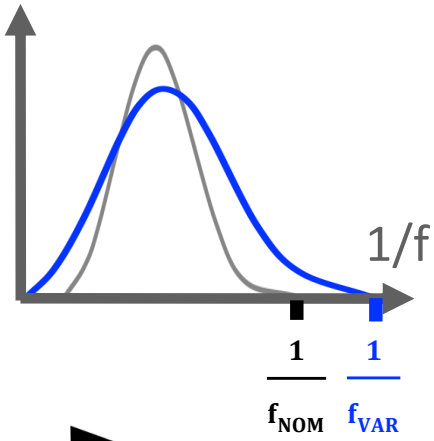

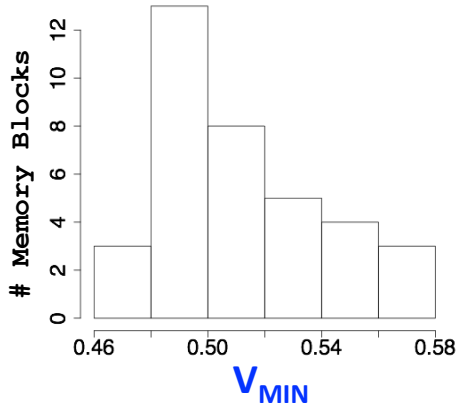

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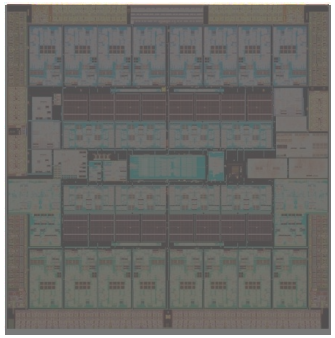

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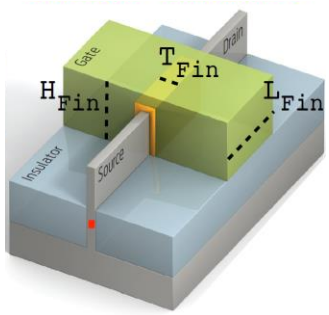

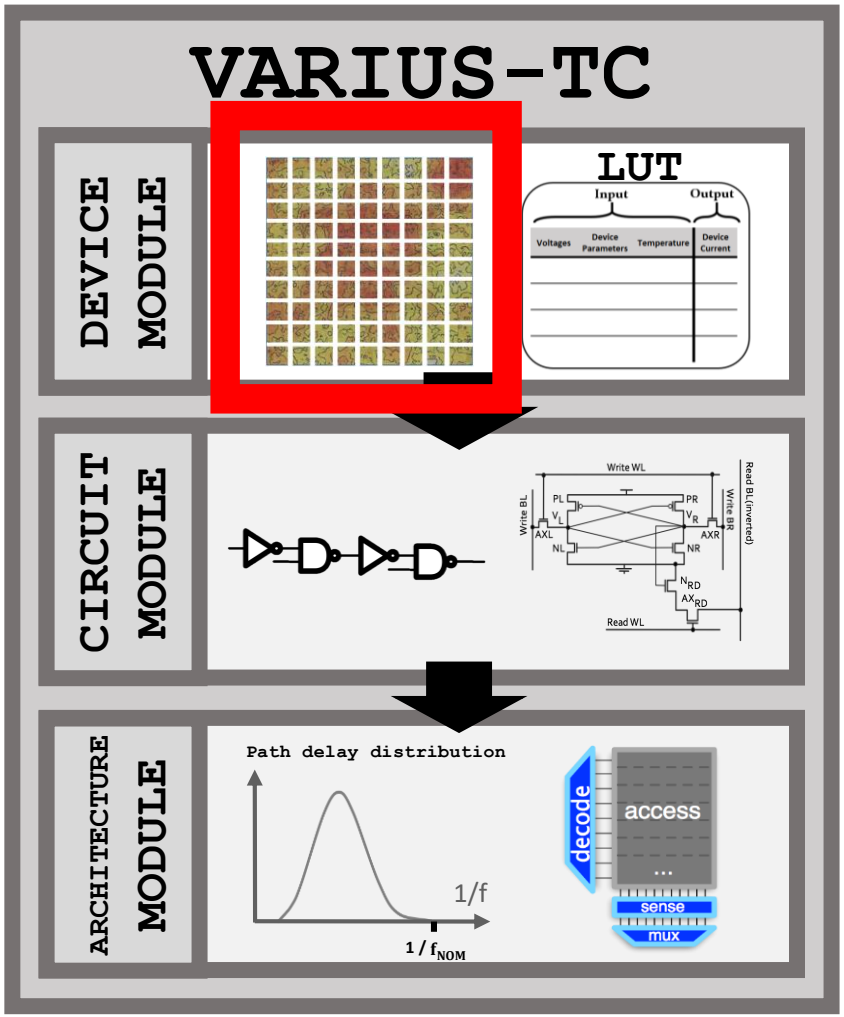

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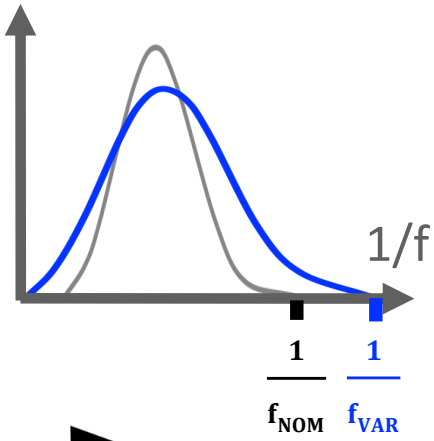

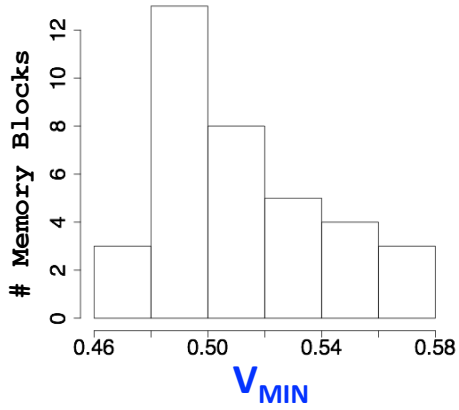

Hierarchical Variation Modeling

Systematic variation

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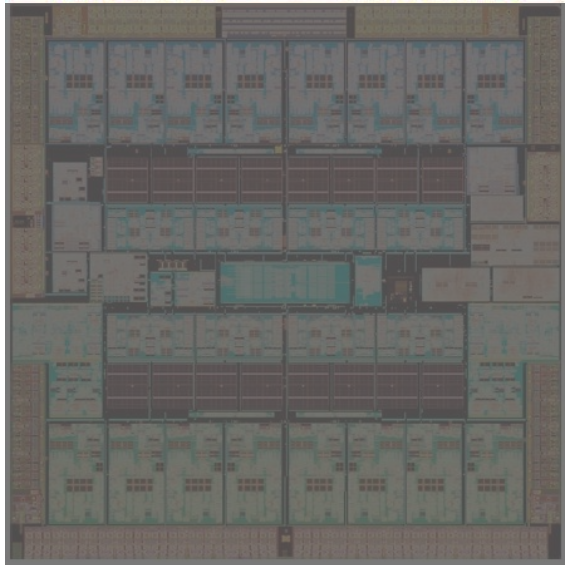

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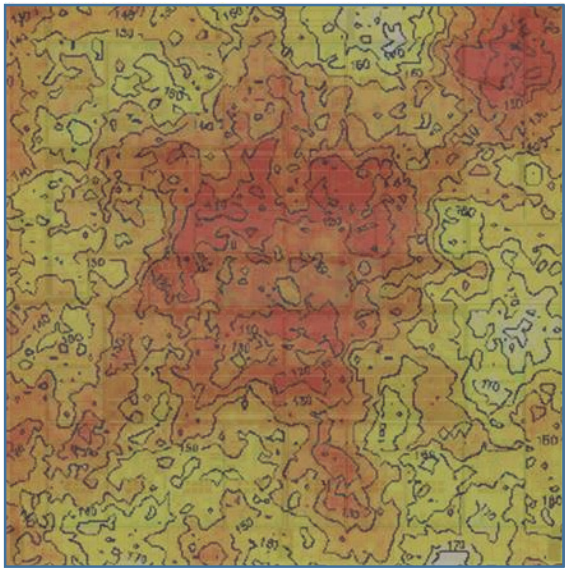
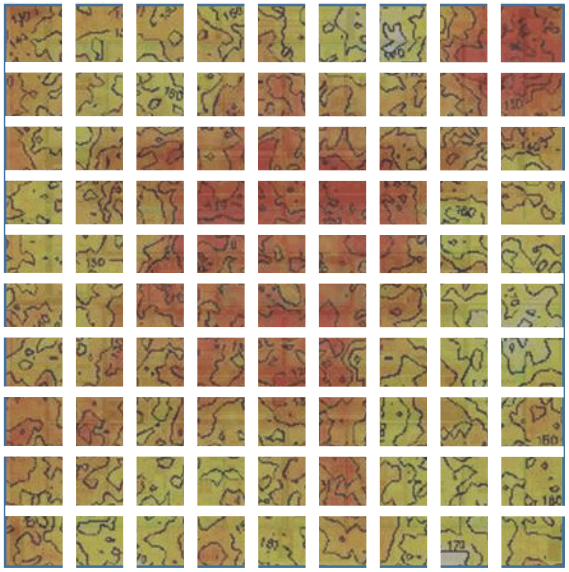


Hierarchical Variation Modeling

Systematic variation

- Spatial correlation
- Grid granularity



Hierarchical Variation Modeling

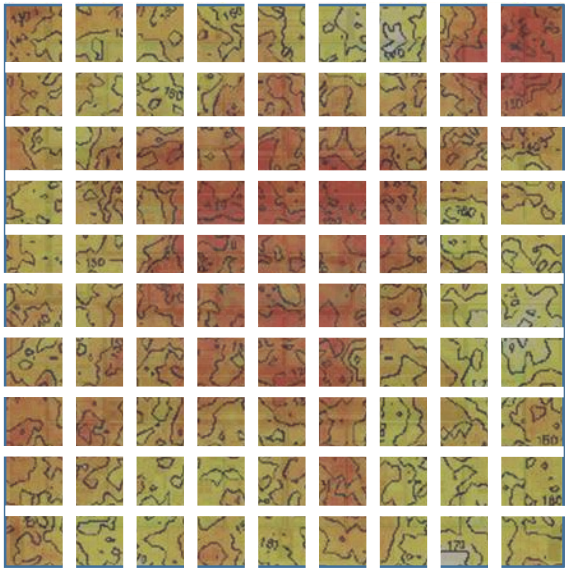
Systematic variation

- Spatial correlation
- Grid granularity

+

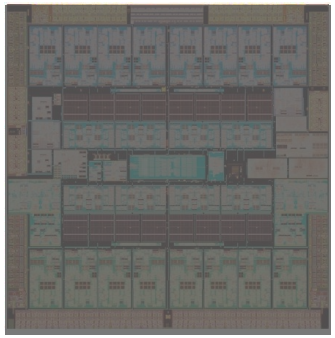
Random variation

- Independent
- Device granularity

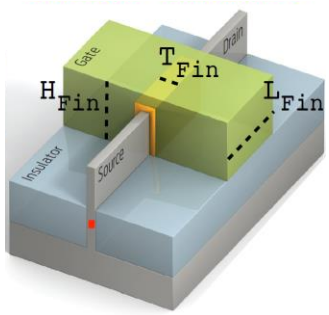


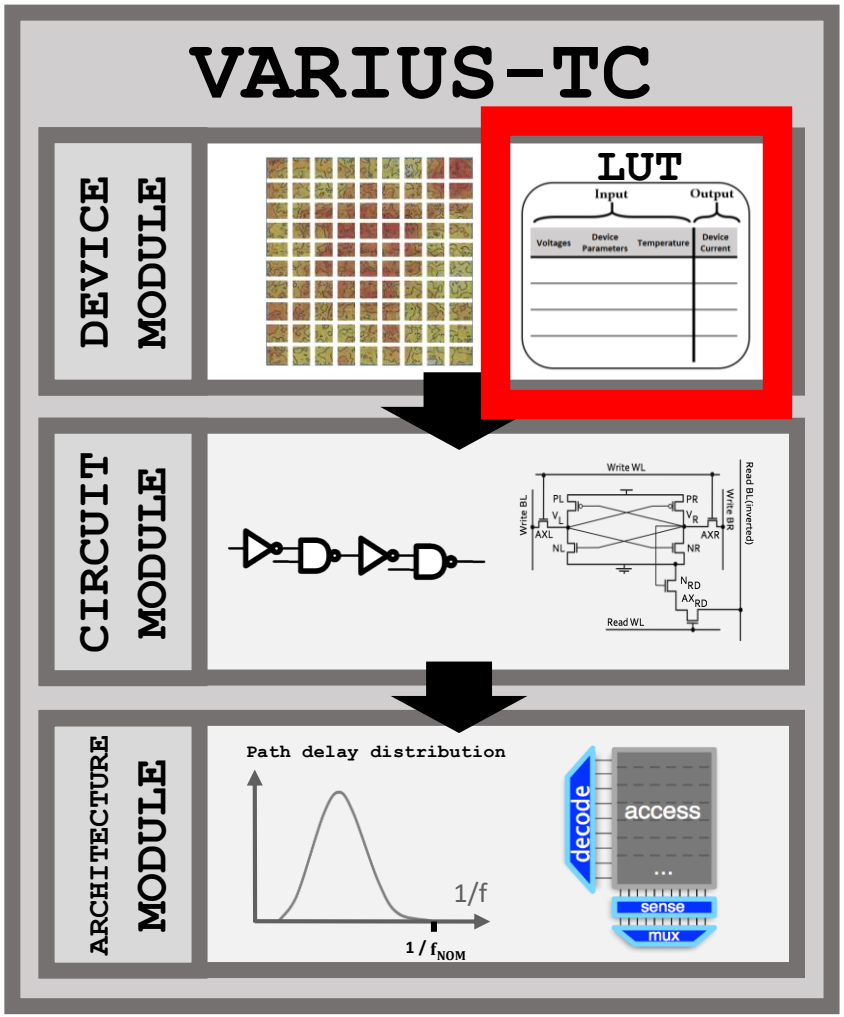
VARIUS-TC: Overview

floorplan



device parameters





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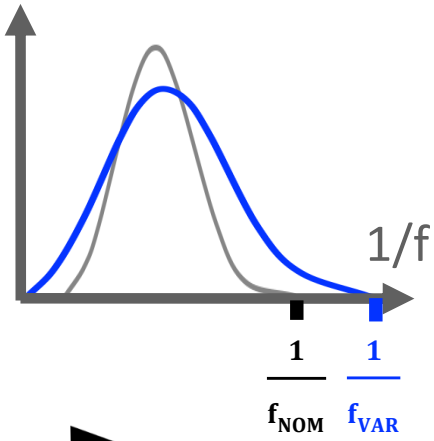

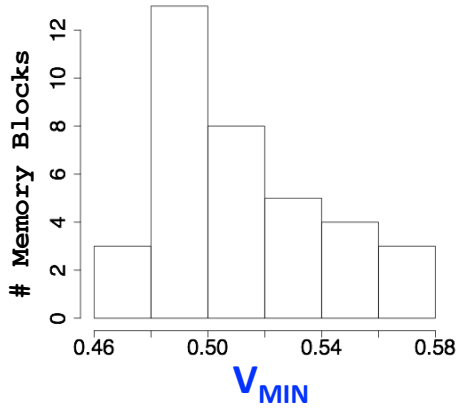

Look-Up Table

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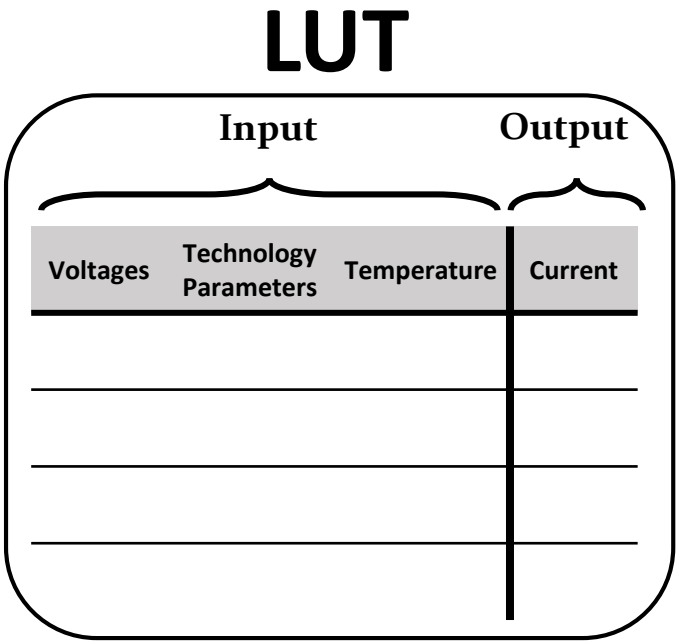

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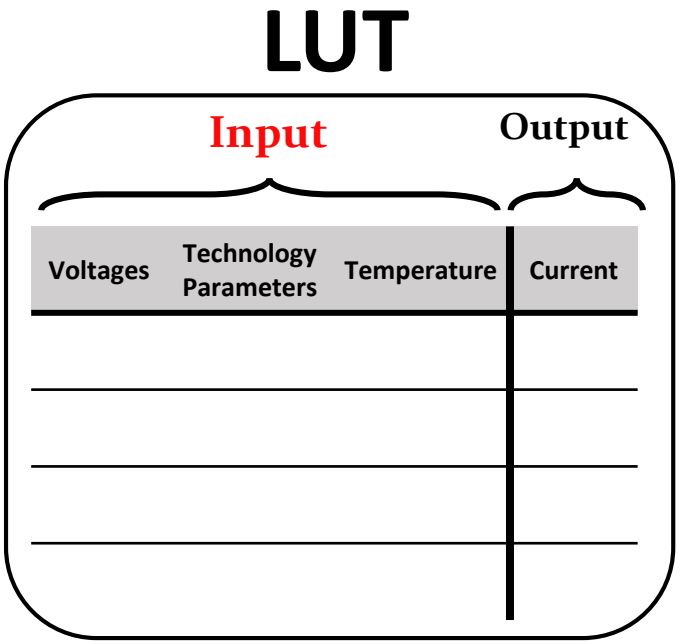

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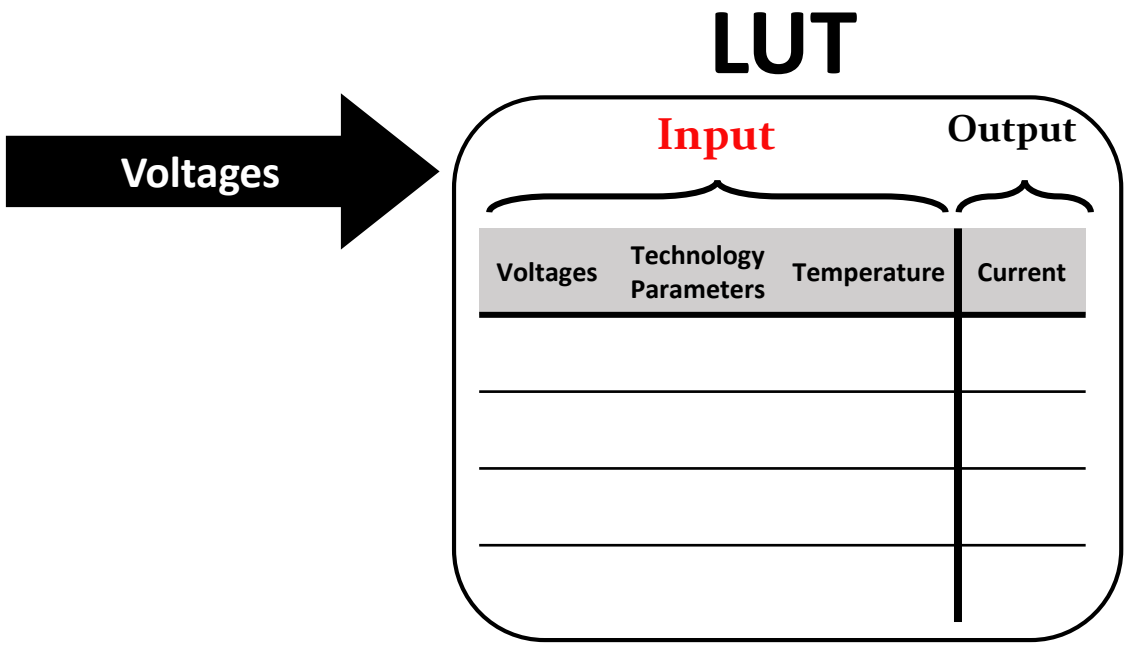

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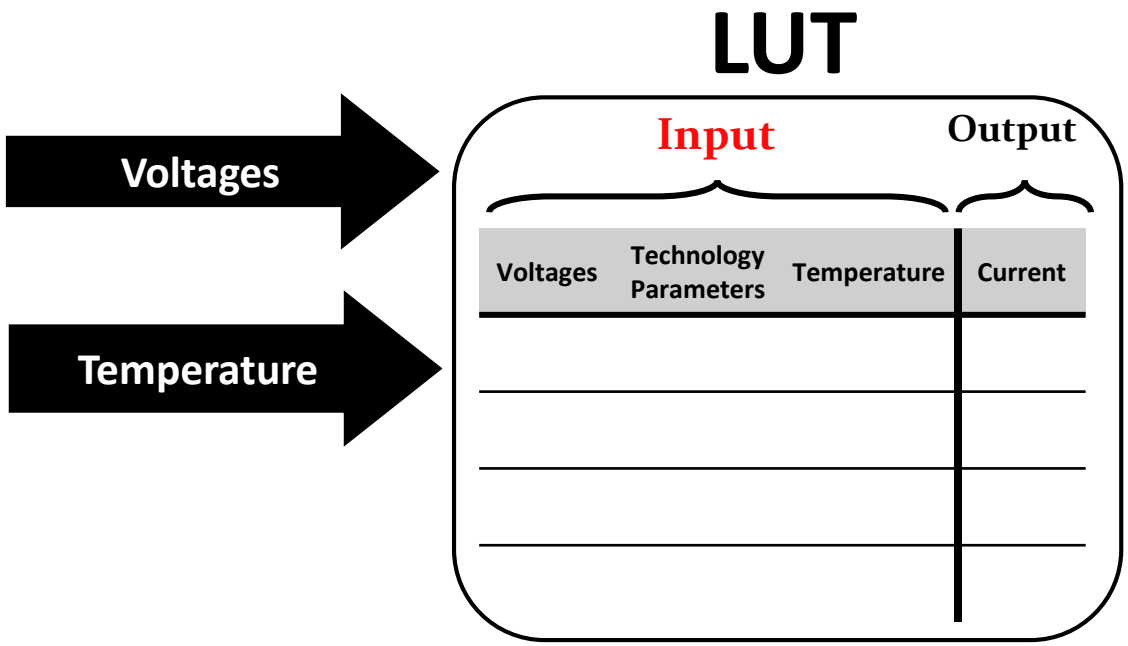

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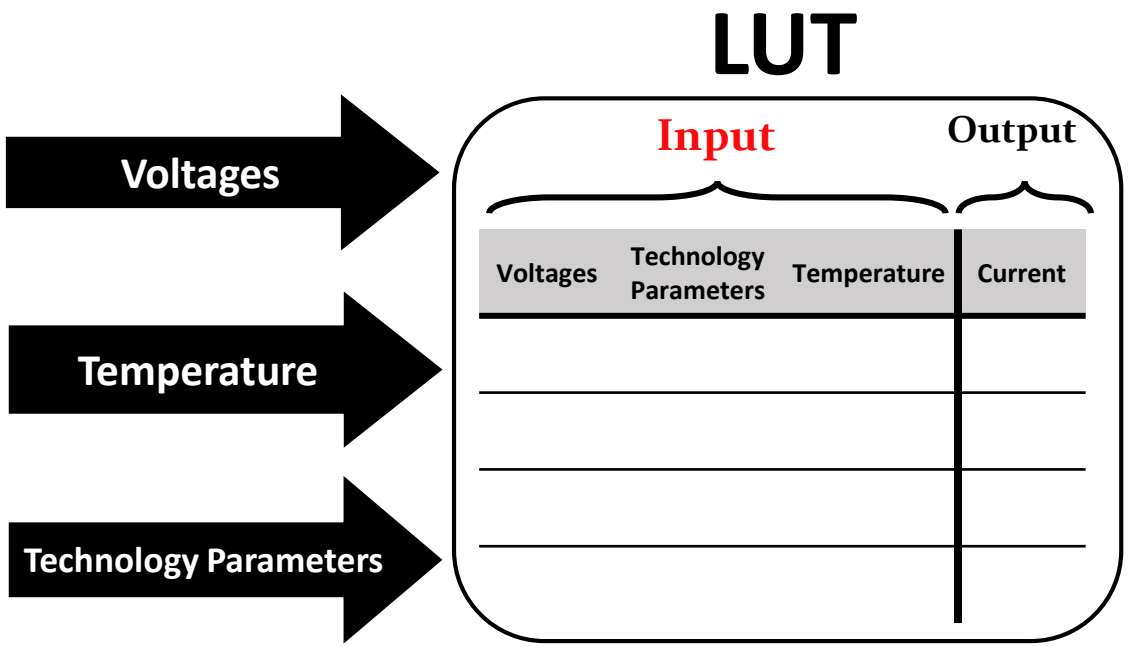

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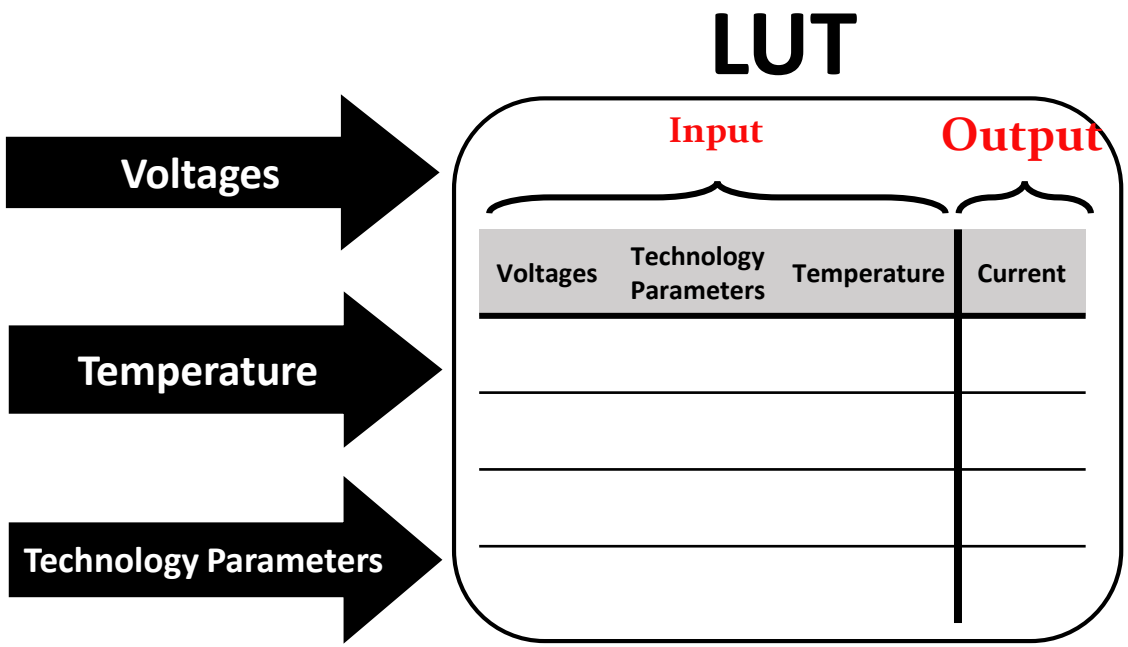

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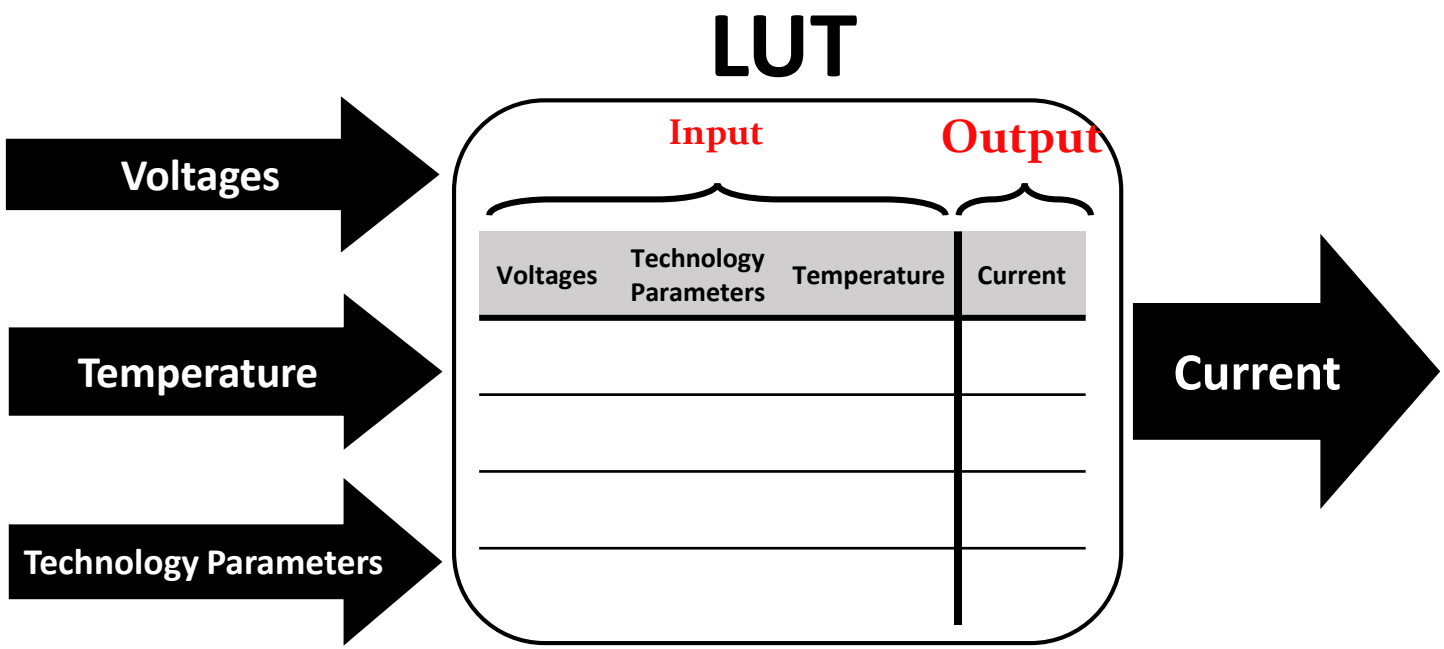

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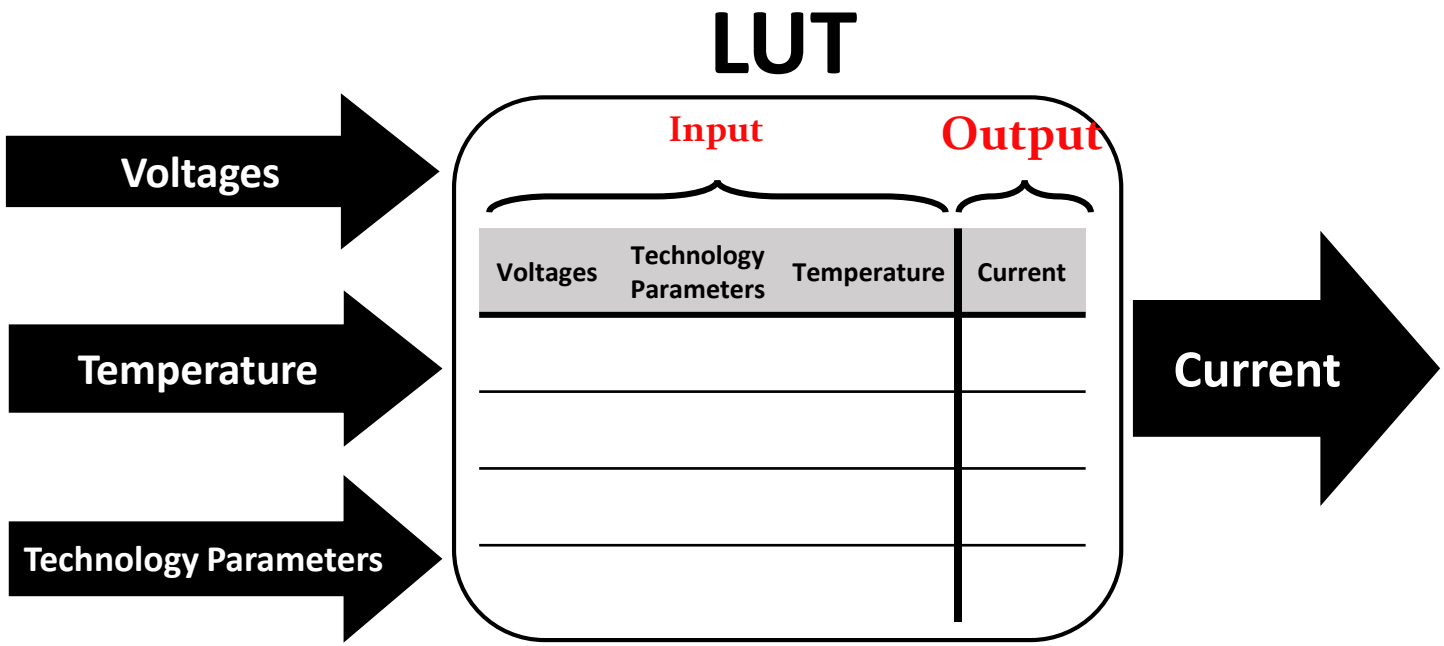

- LUT vs. closed-form formula:

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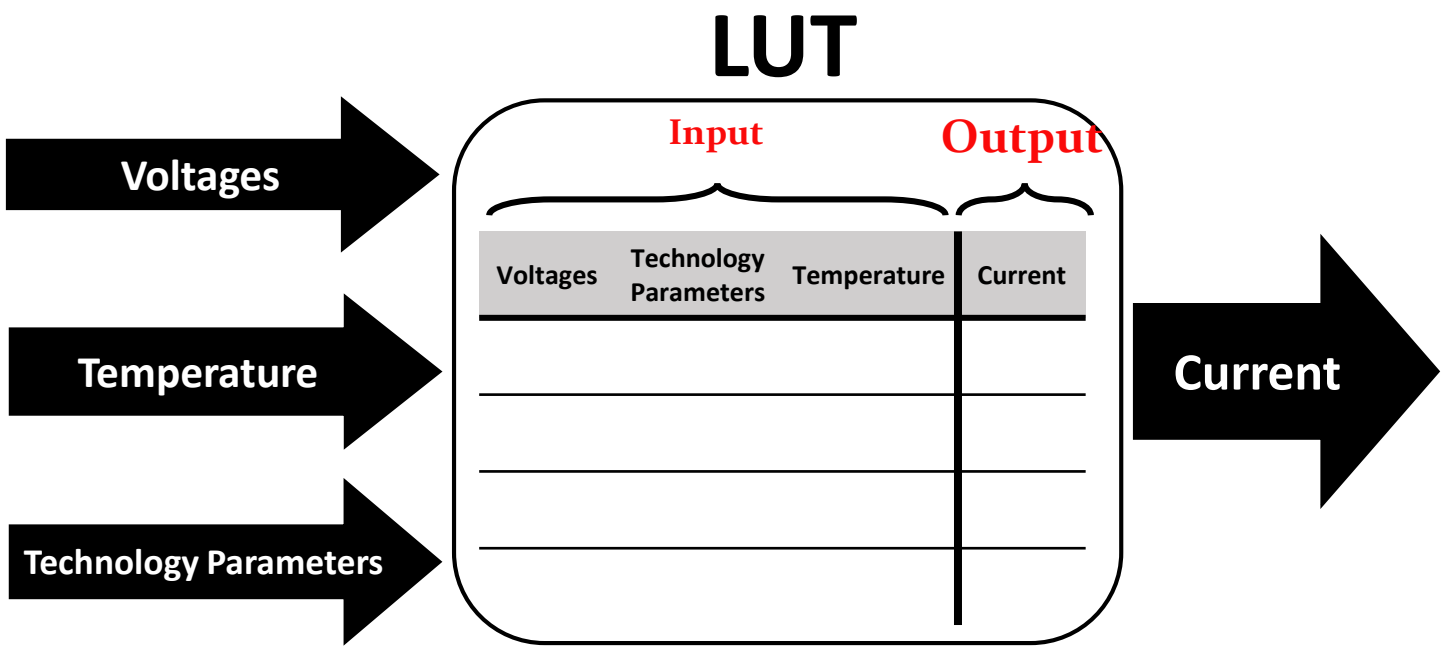

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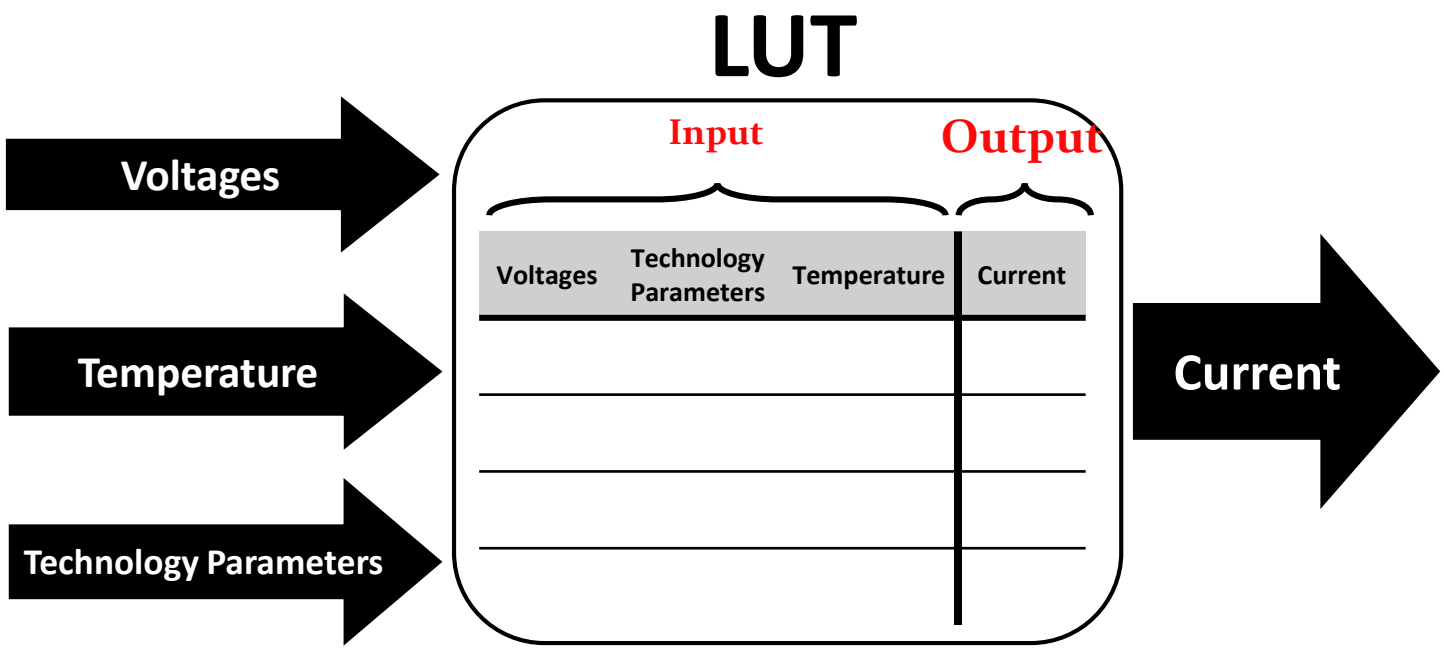

- LUT vs. closed-form formula:
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  - Robust closed-form formula may not always be available for emerging switches

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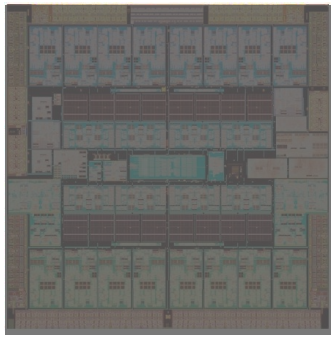
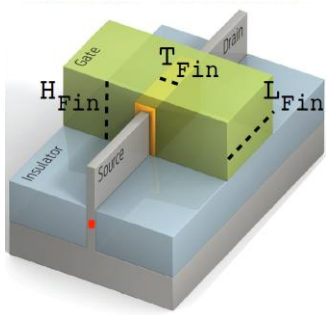
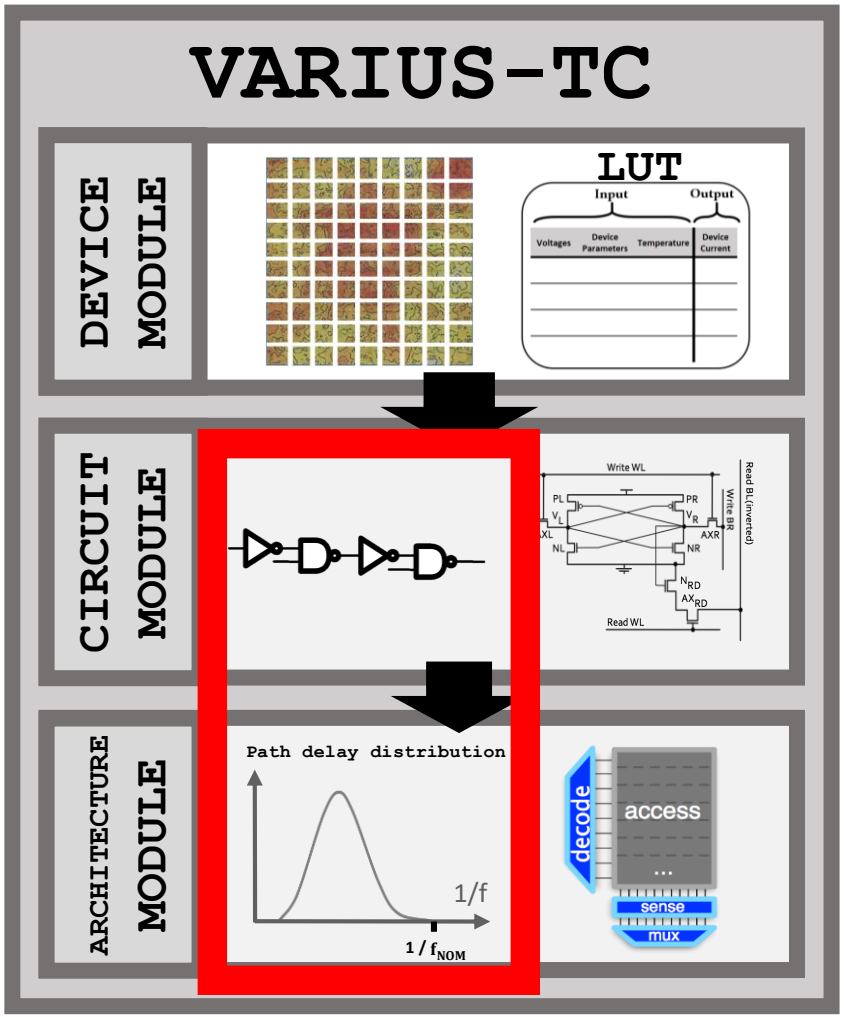
floorplan

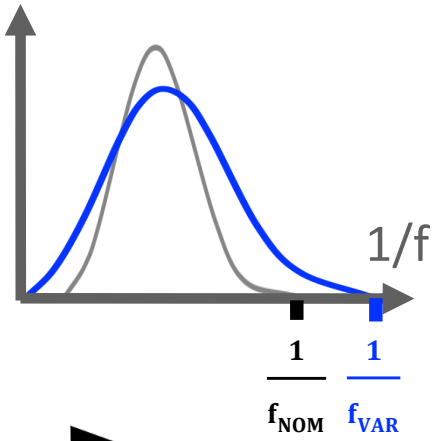


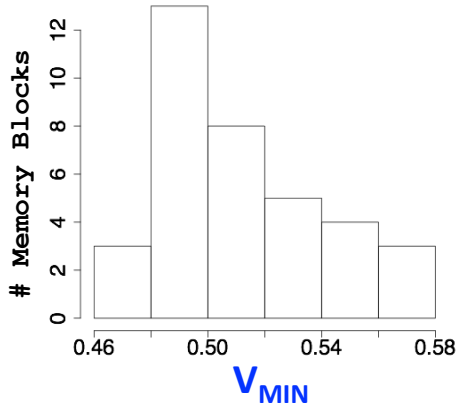
device parameters





Path delay distribution





Logic Timing Model

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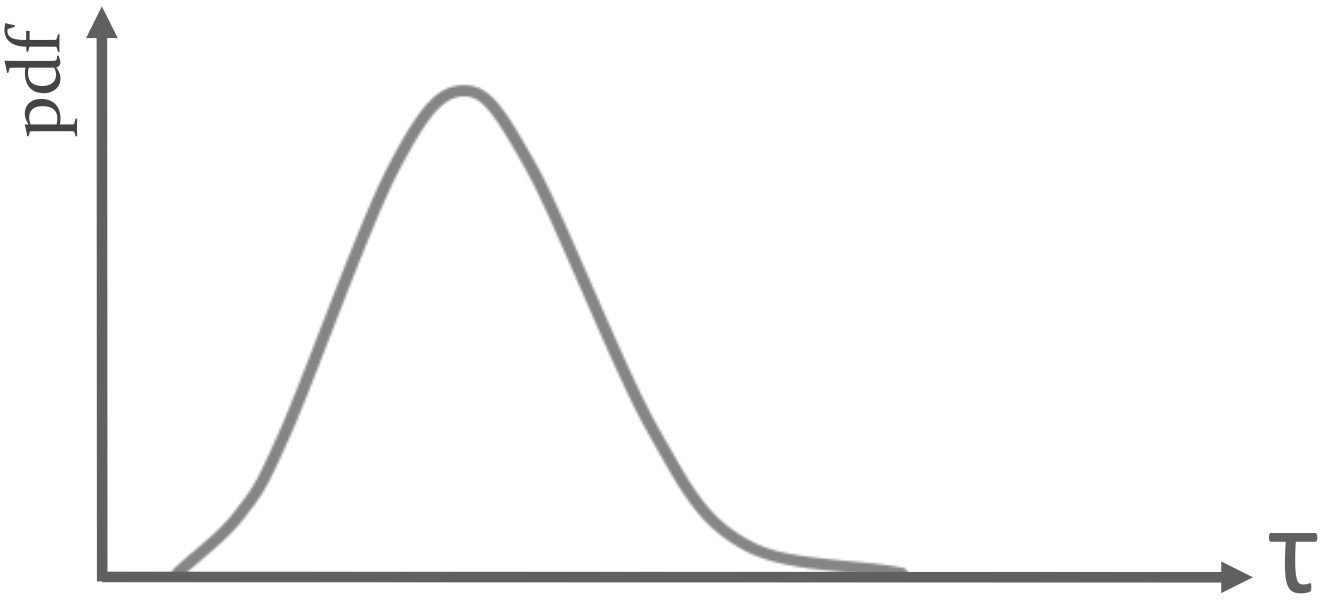
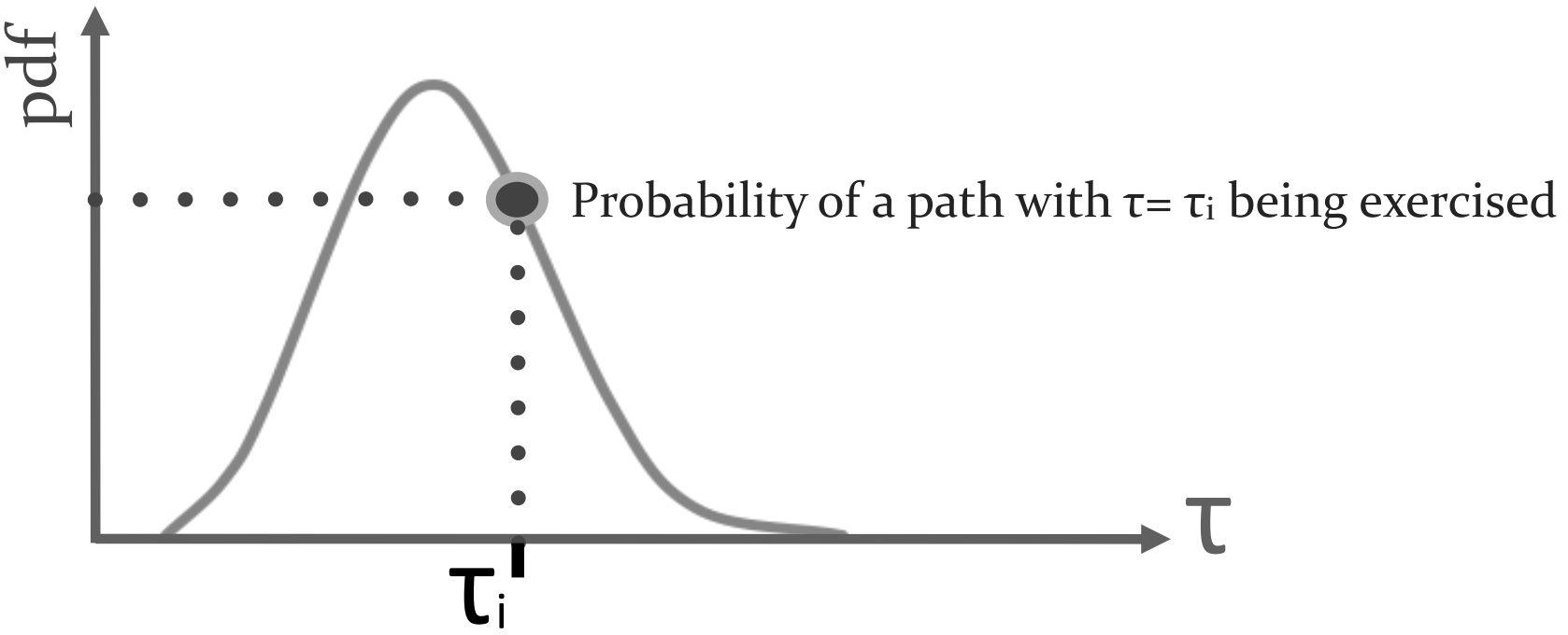
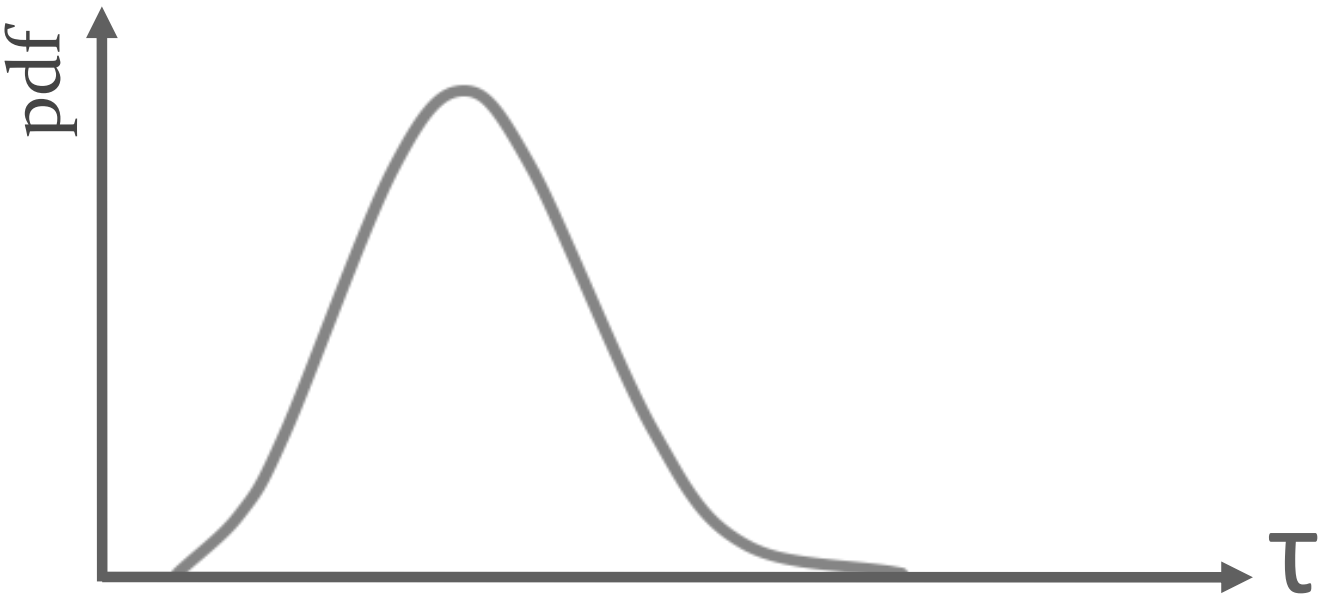


Logic Timing Model



Logic Timing Model



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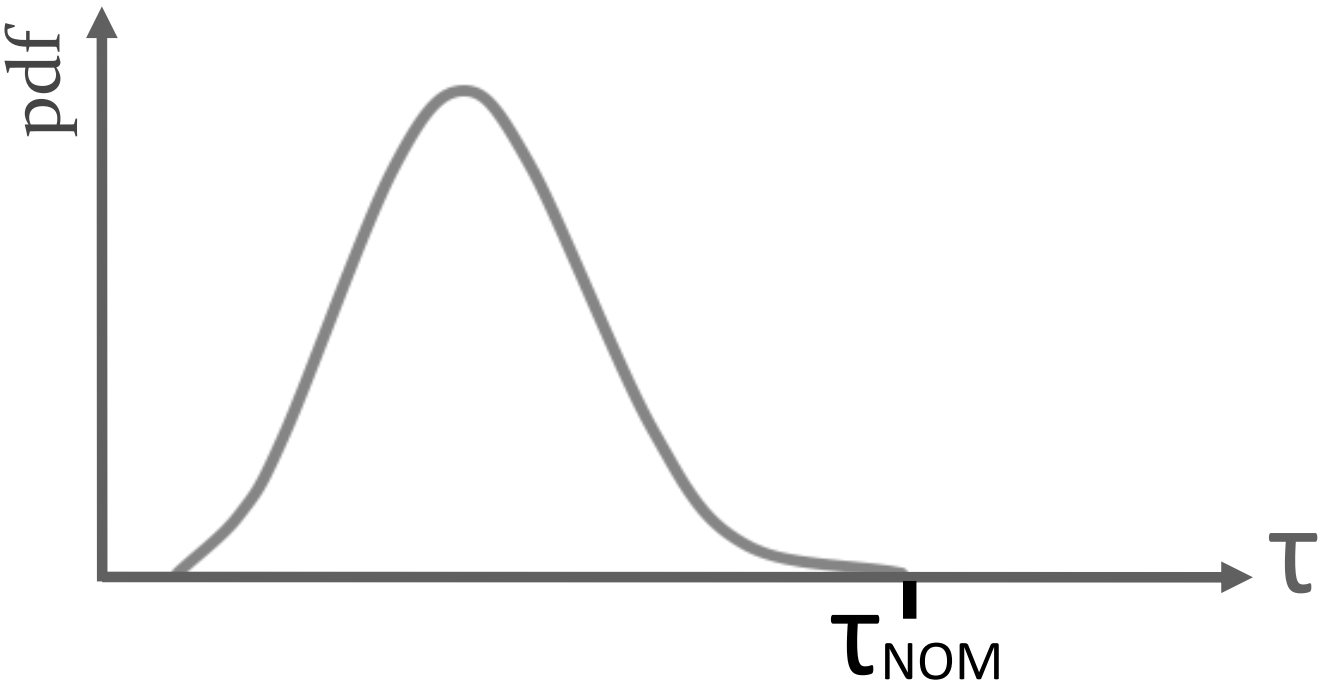

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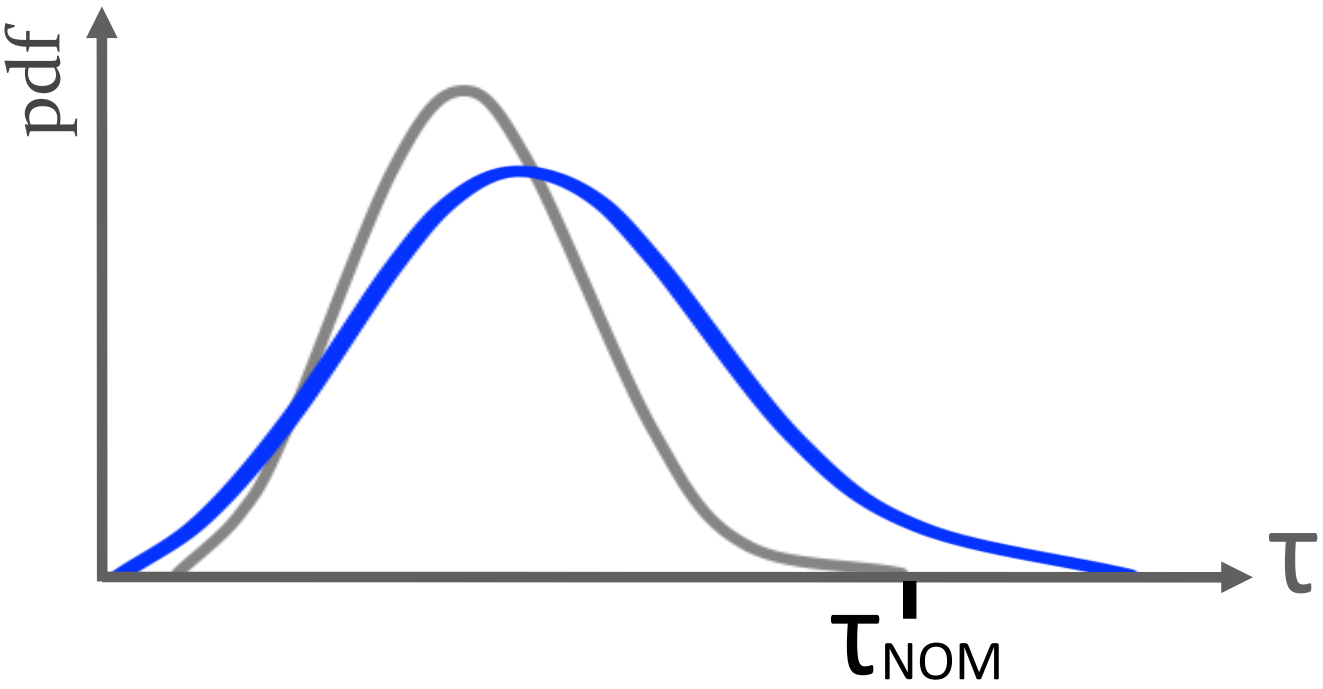
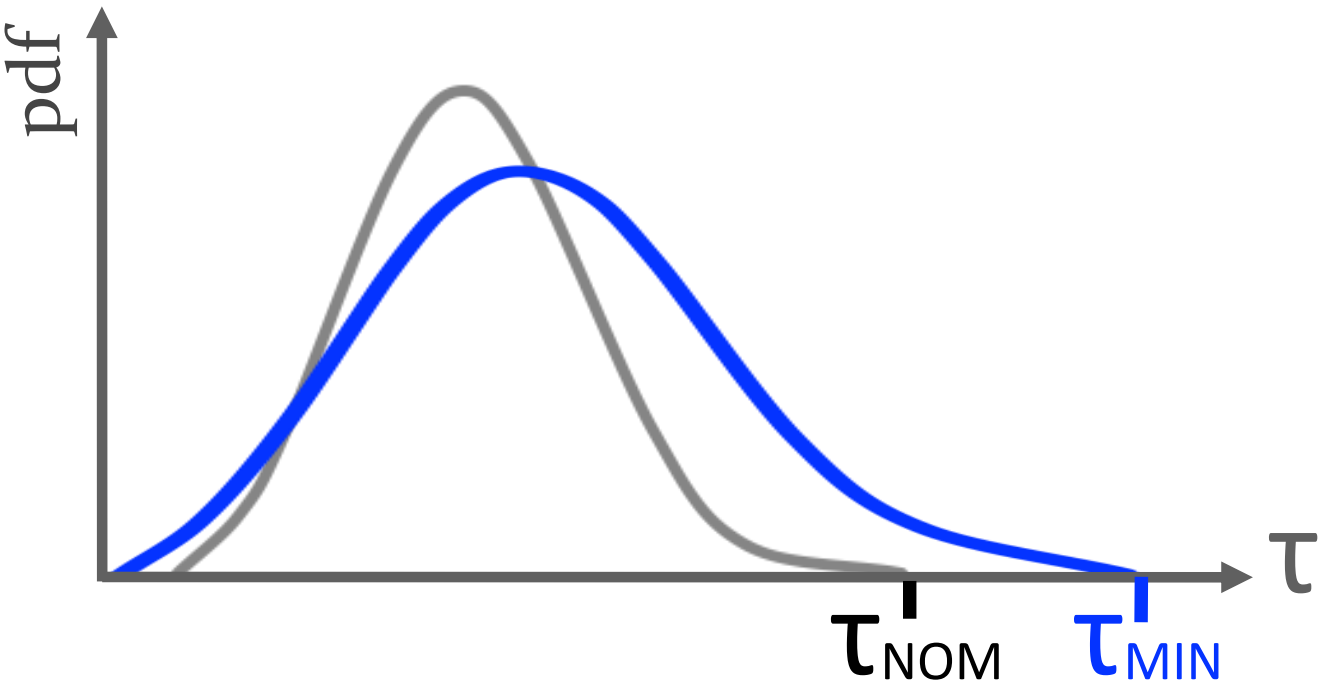


Logic Timing Model



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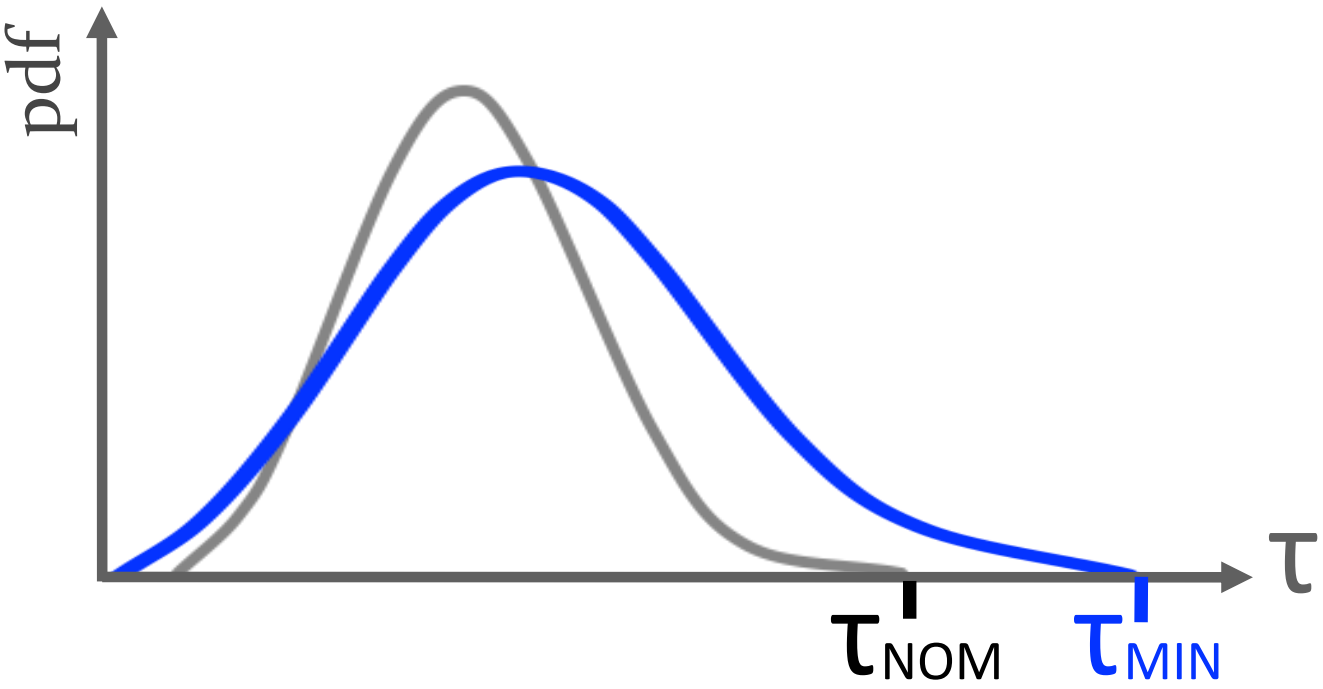
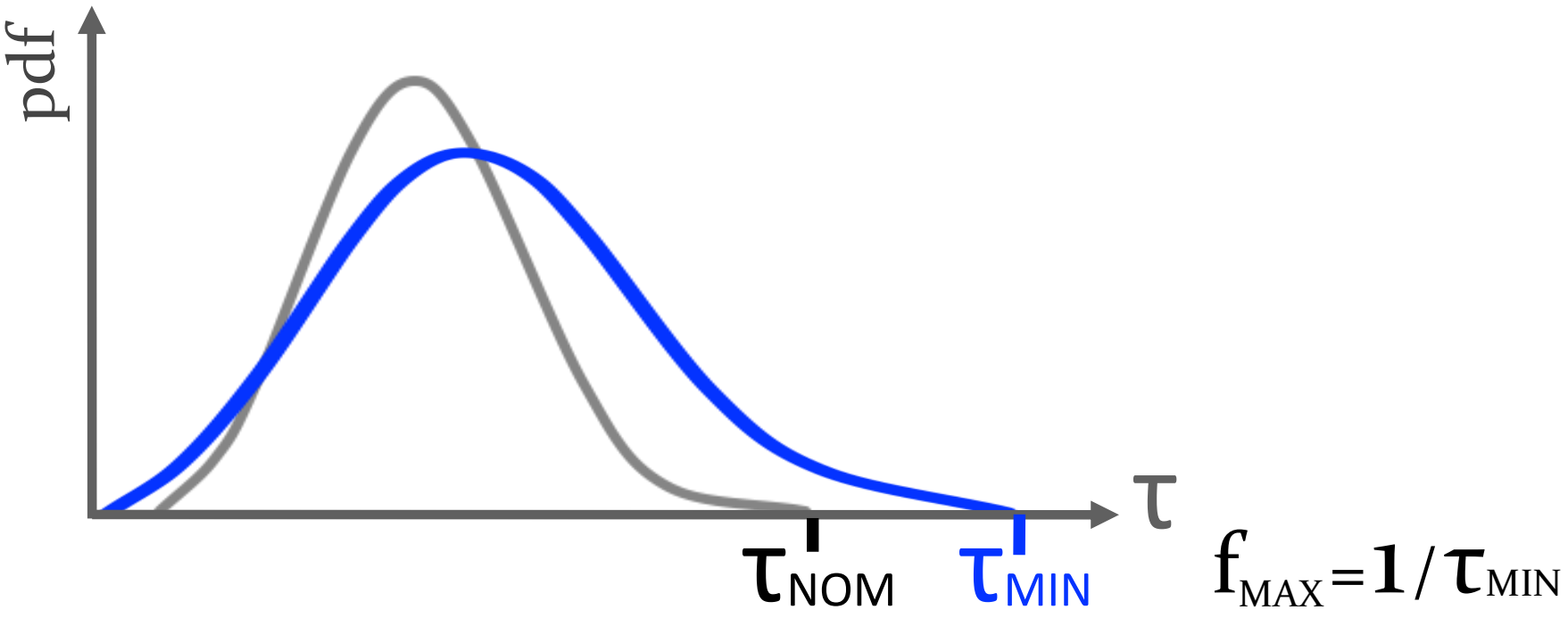
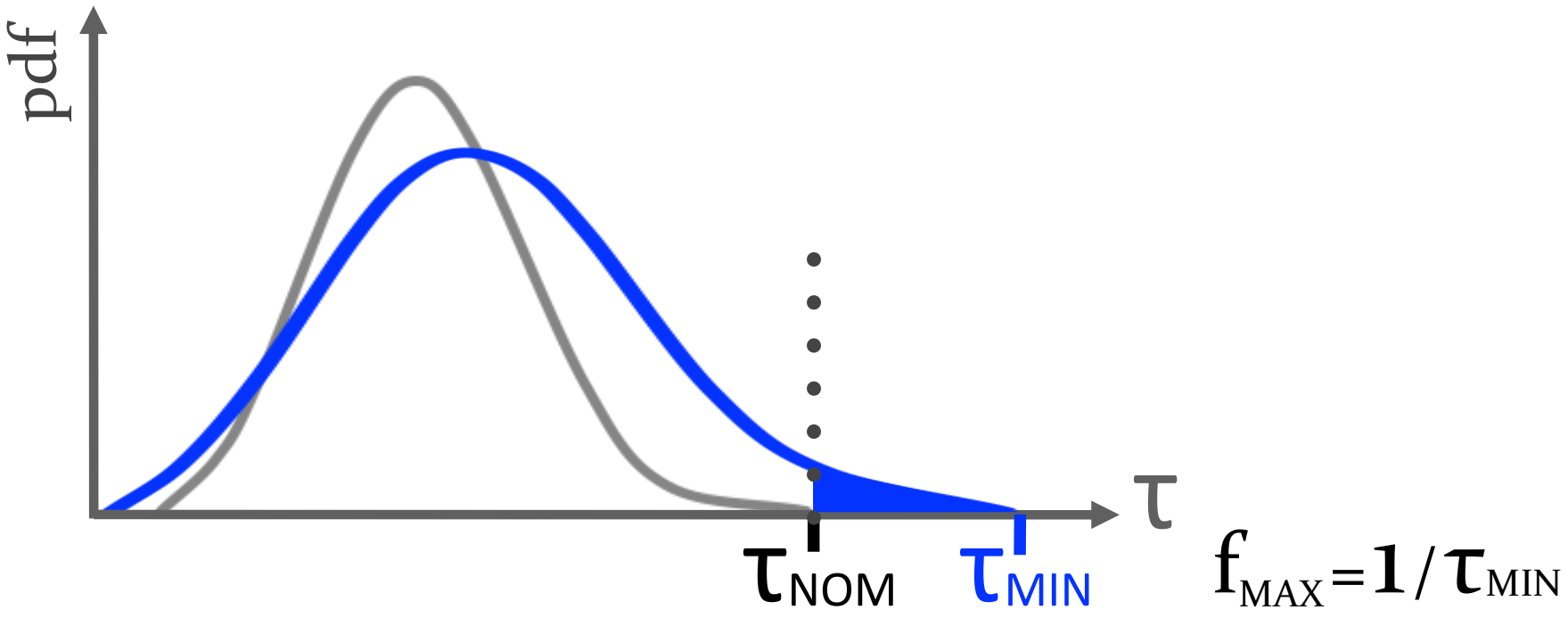


Safe operating point

Logic Timing Model



Logic Timing Model



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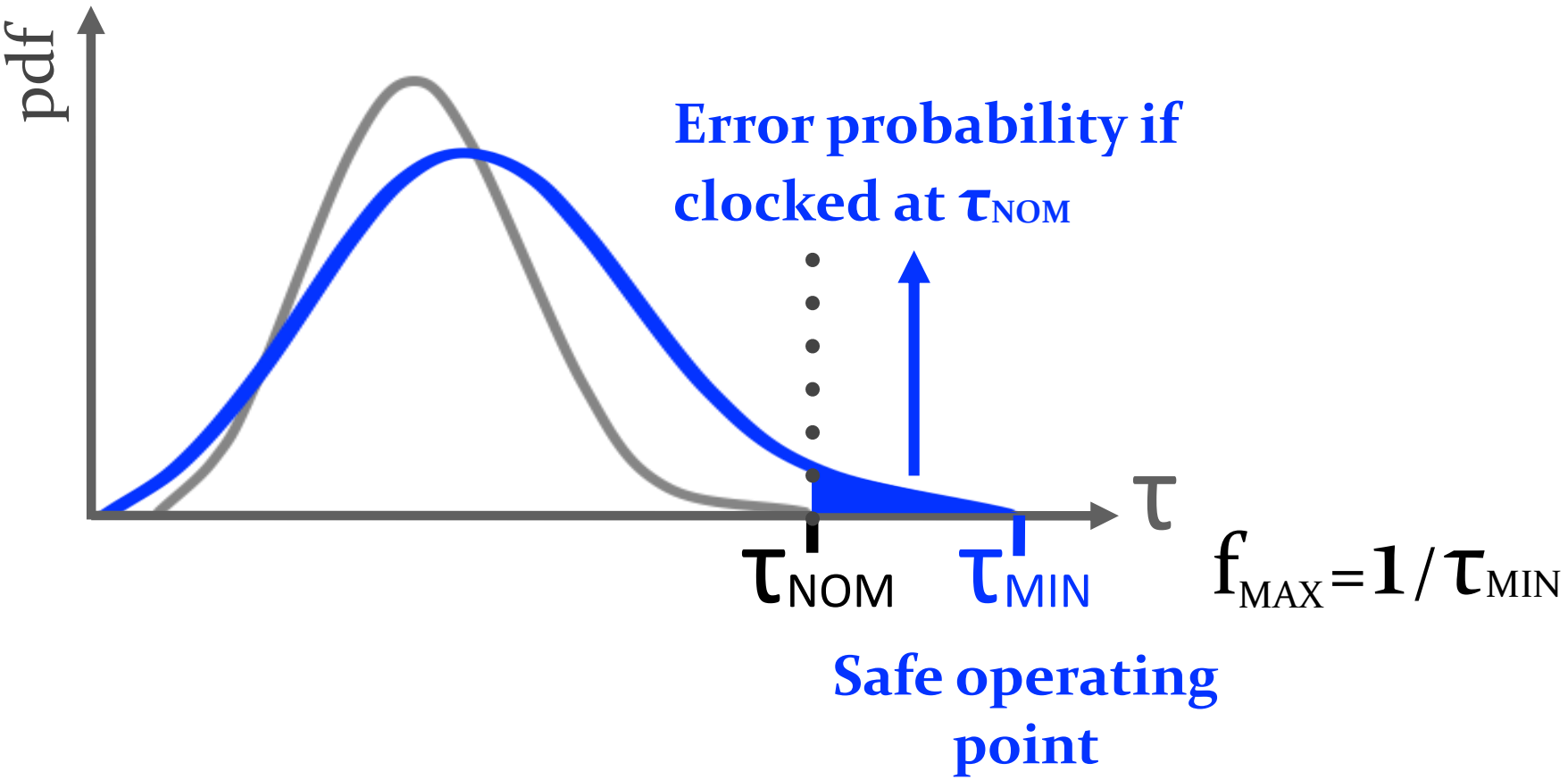
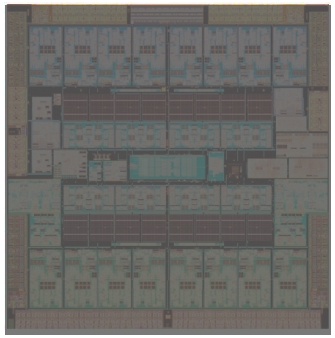
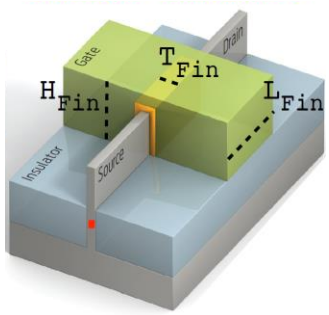


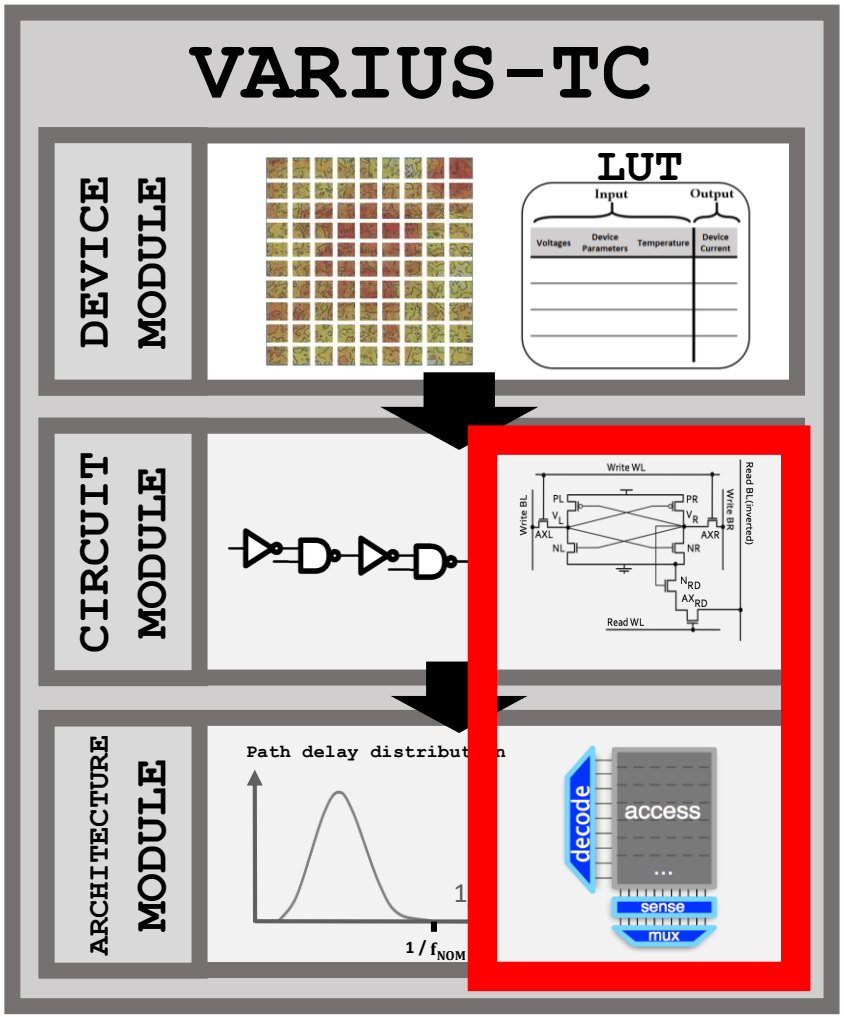
VARIUS-TC: Overview

floorplan



device parameters





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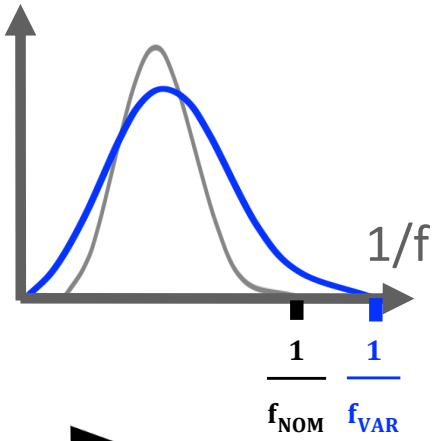

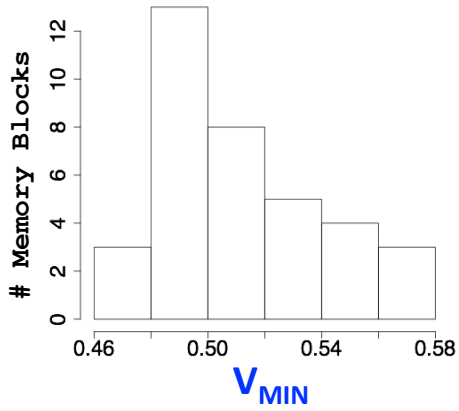

Memory Model

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- Supports 6T and 8T memory cell

Memory Model

- Supports 6T and 8T memory cell
- Timing errors
  - Write timing
  - Read timing

Memory Model

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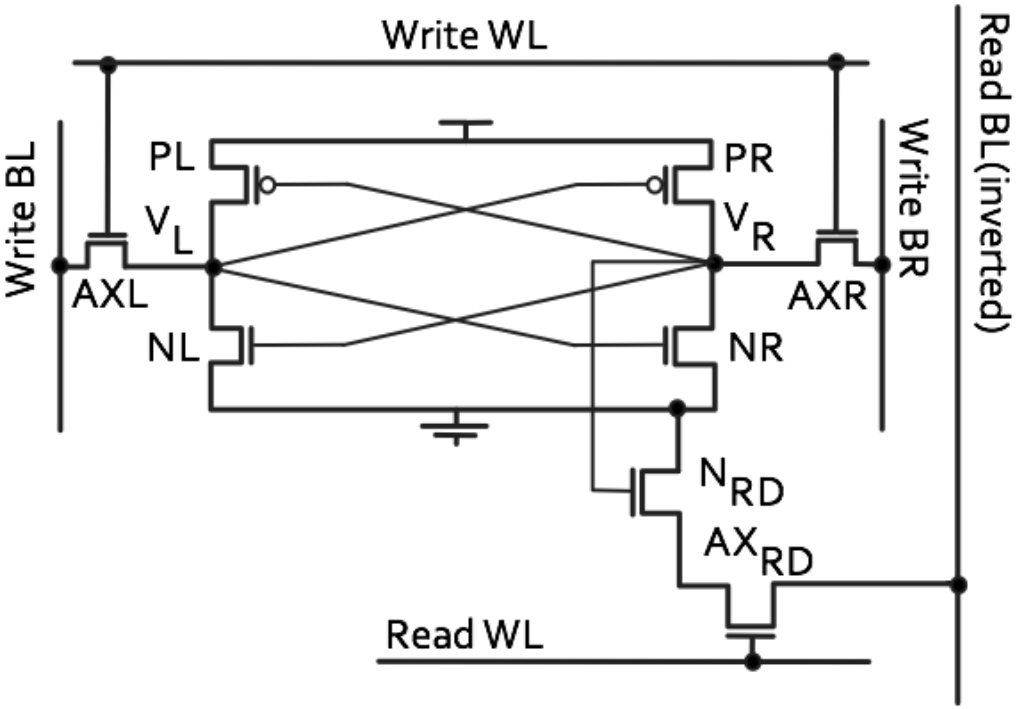
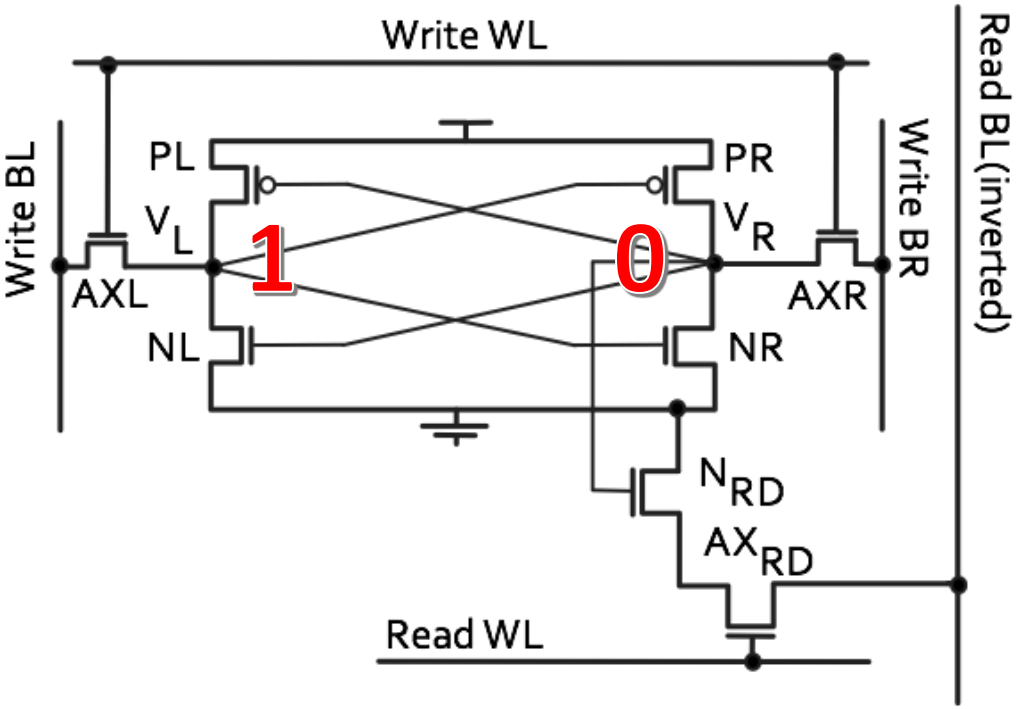
- Timing errors
  - Write timing
  - Read timing
- Stability errors
  - Hold error
  - Write Stability

Hold Error

Hold Error

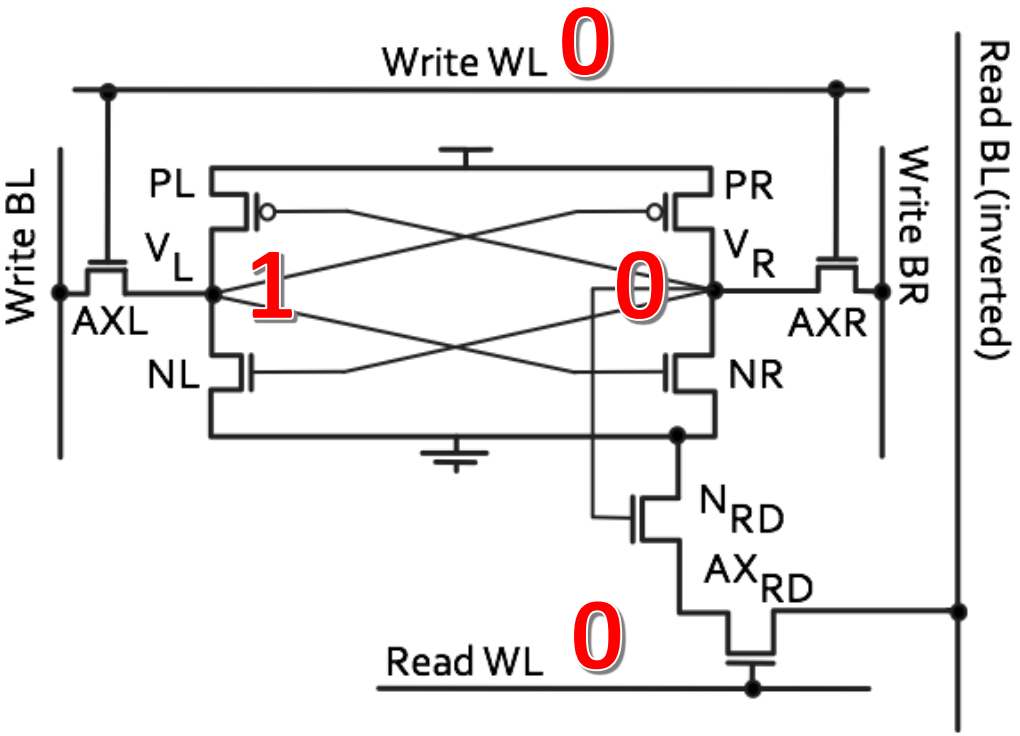

Write WL
Read BL(inverted)
Write BL
Write BR
PL
PR
V_L
V_R
AXL
AXR
NL
NR
N_{RD}
AX_{RD}
Read WL

Hold Error


Write WL
Write BL
PL
PR
V_L
V_R
1
0
AXL
AXR
Write BR
NL
NR
N_{RD}
AX_{RD}
Read BL(inverted)
Read WL

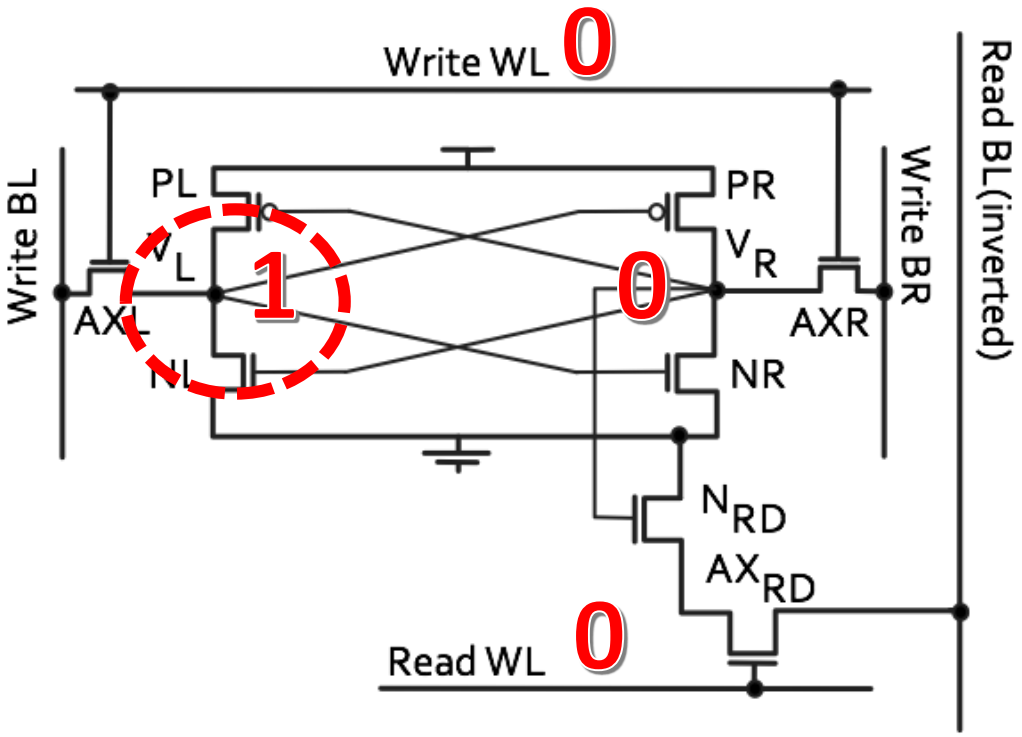
Hold Error

- The cell is not accessed.



Hold Error

- The cell is not accessed.
- Node V_L looses its state.



Hold Error

- The cell is not accessed.
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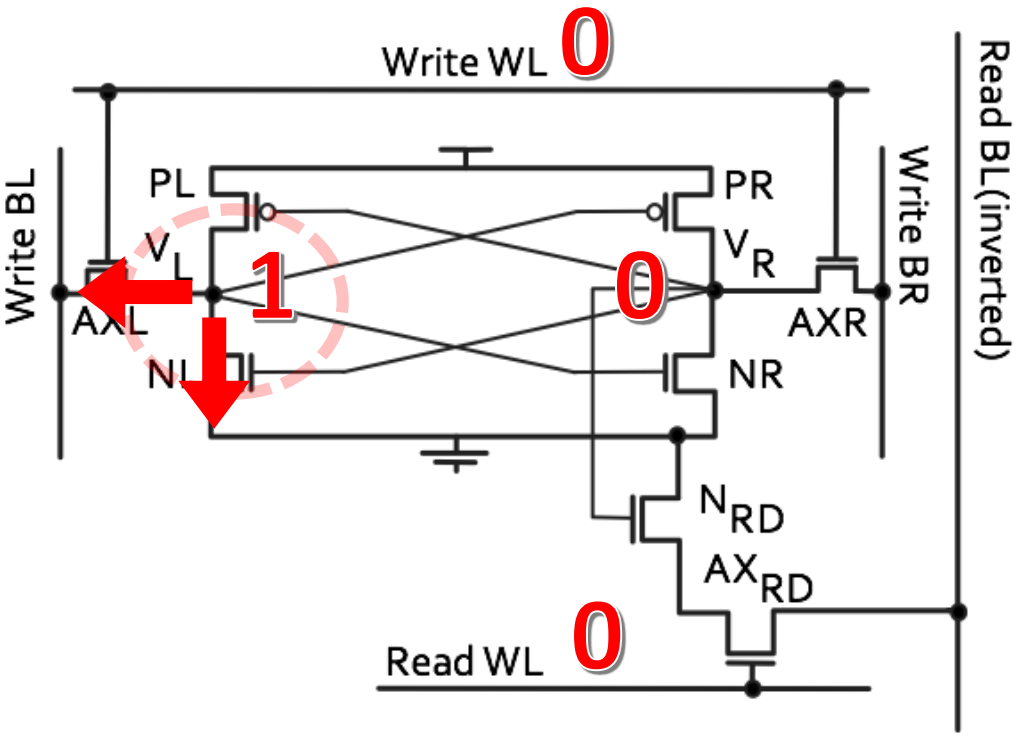

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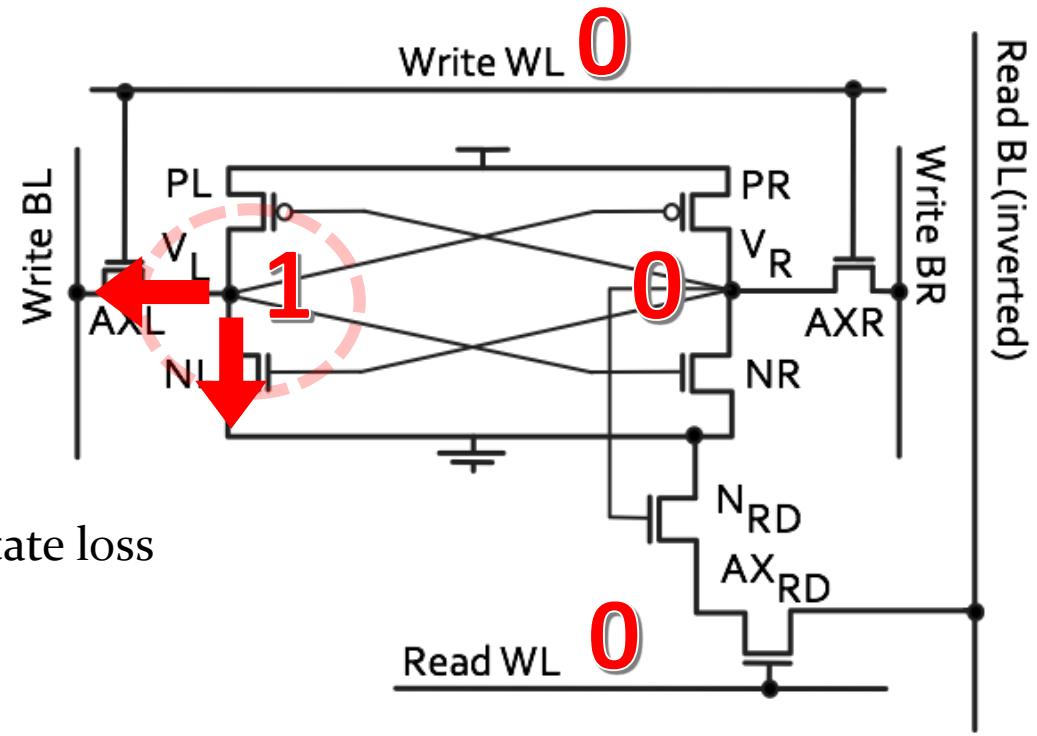

VARIUS-TC

- Minimum Vdd (V_{MIN}) to exclude state loss

Evaluation Setup

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- Device parameters
  - PTM, FinFET, 16nm

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- Parametric sweep
  - L_{Fin}, T_{Fin}, ϕ_g

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  - PTM, FinFET, 16nm
- Parametric sweep
  - L_{Fin}, T_{Fin}, ϕ_g
- 3 levels of variation
  - low, medium, high

Parameter	Low var.	Medium var.	High var.
L_{Fin}	3.5%	7%	10.5%
T_{Fin}	3.5%	7%	10.5%
ϕ_g	0.16%	0.32%	0.48%

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- Device parameters
  - PTM, FinFET, 16nm
- Parametric sweep
  - L_{Fin}, T_{Fin}, ϕ_g
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  - low, medium, high
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  - 16 tiles

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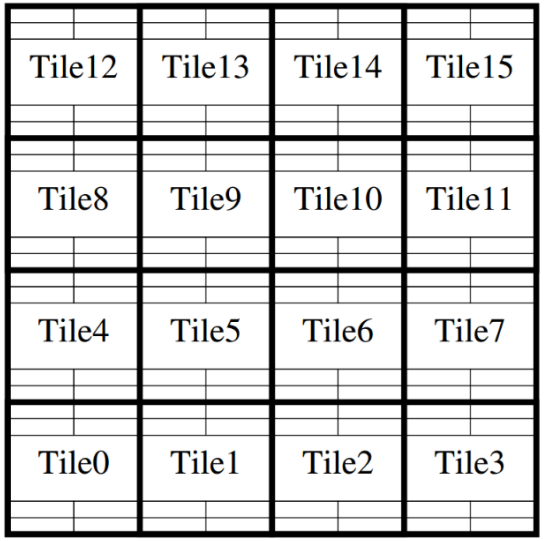

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- Parametric sweep
  - L_{Fin}, T_{Fin}, ϕ_g
- 3 levels of variation
  - low, medium, high
- Many-core system
  - 16 tiles
  - 4 core per tile
  - Private L1, Shared L2

Parameter	Low var.	Medium var.	High var.
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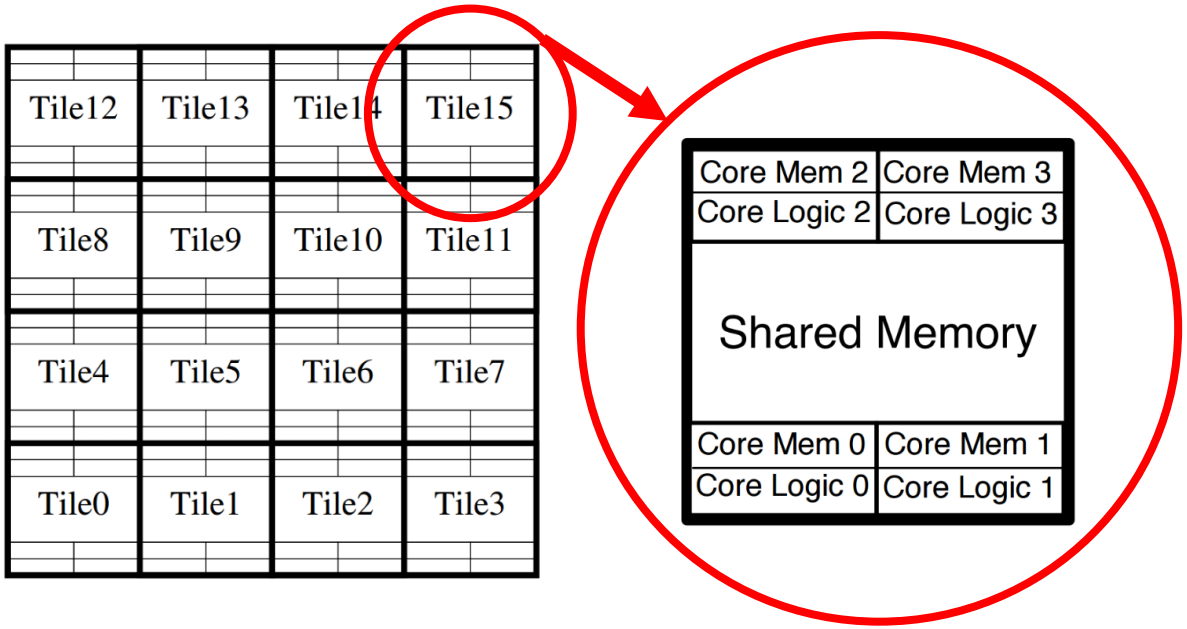

Impact on Logic Timing

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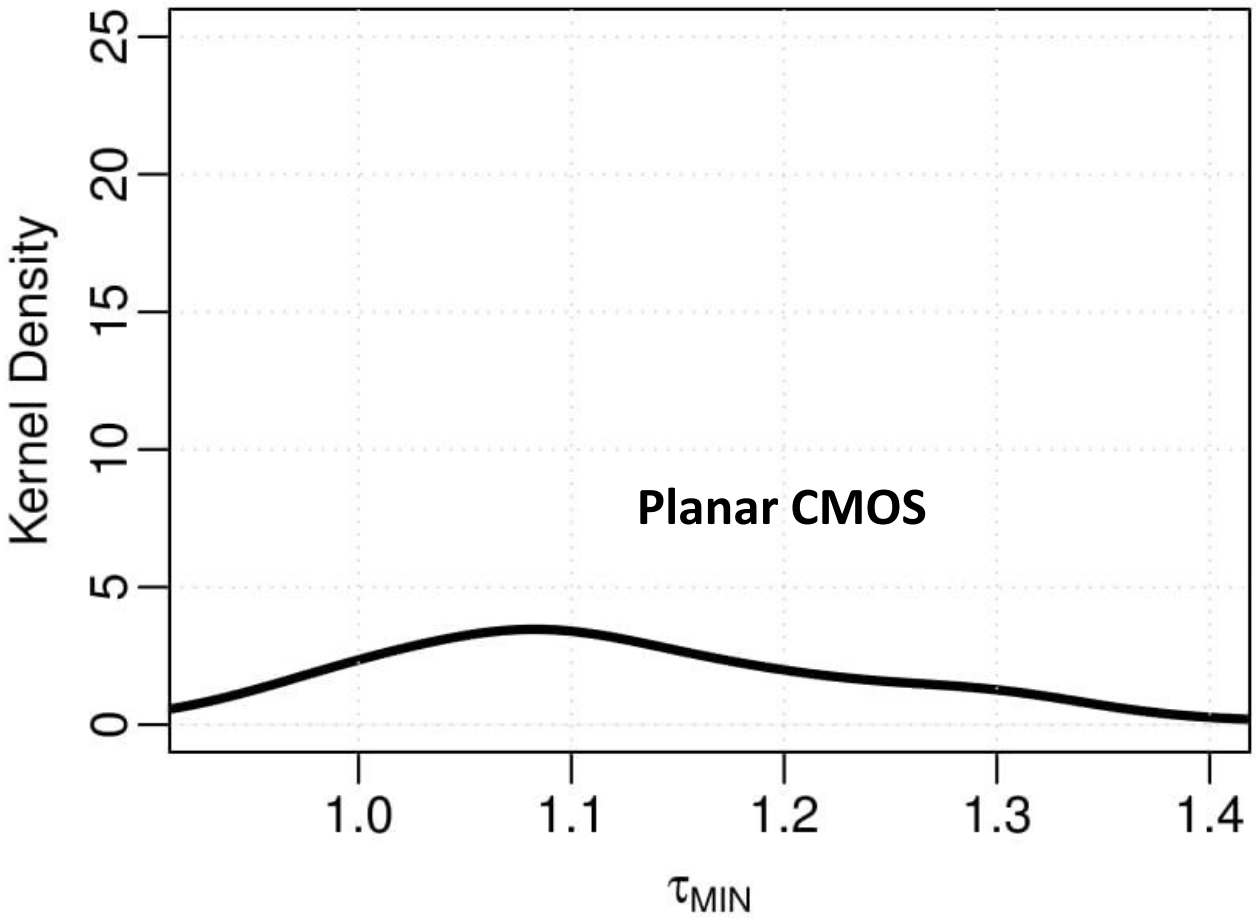

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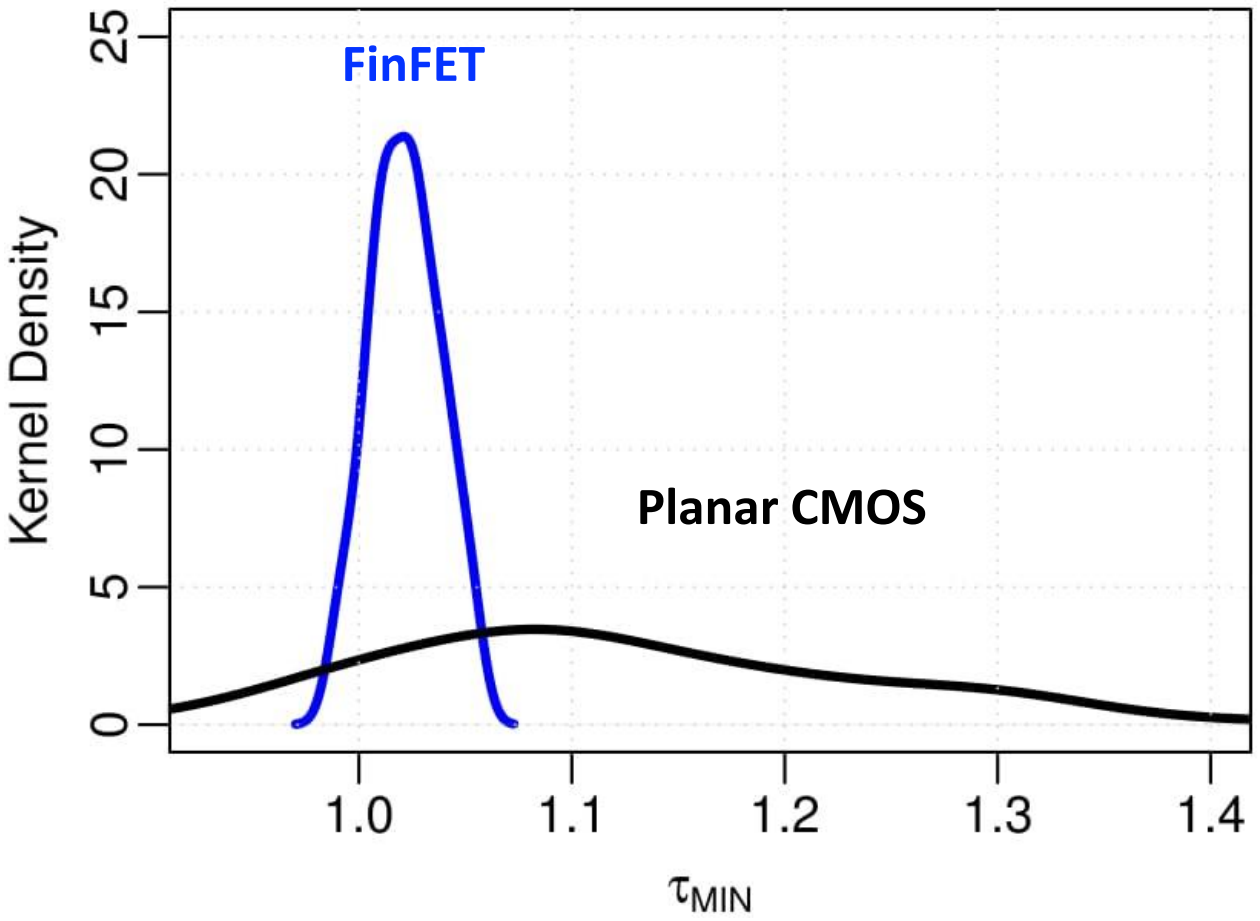

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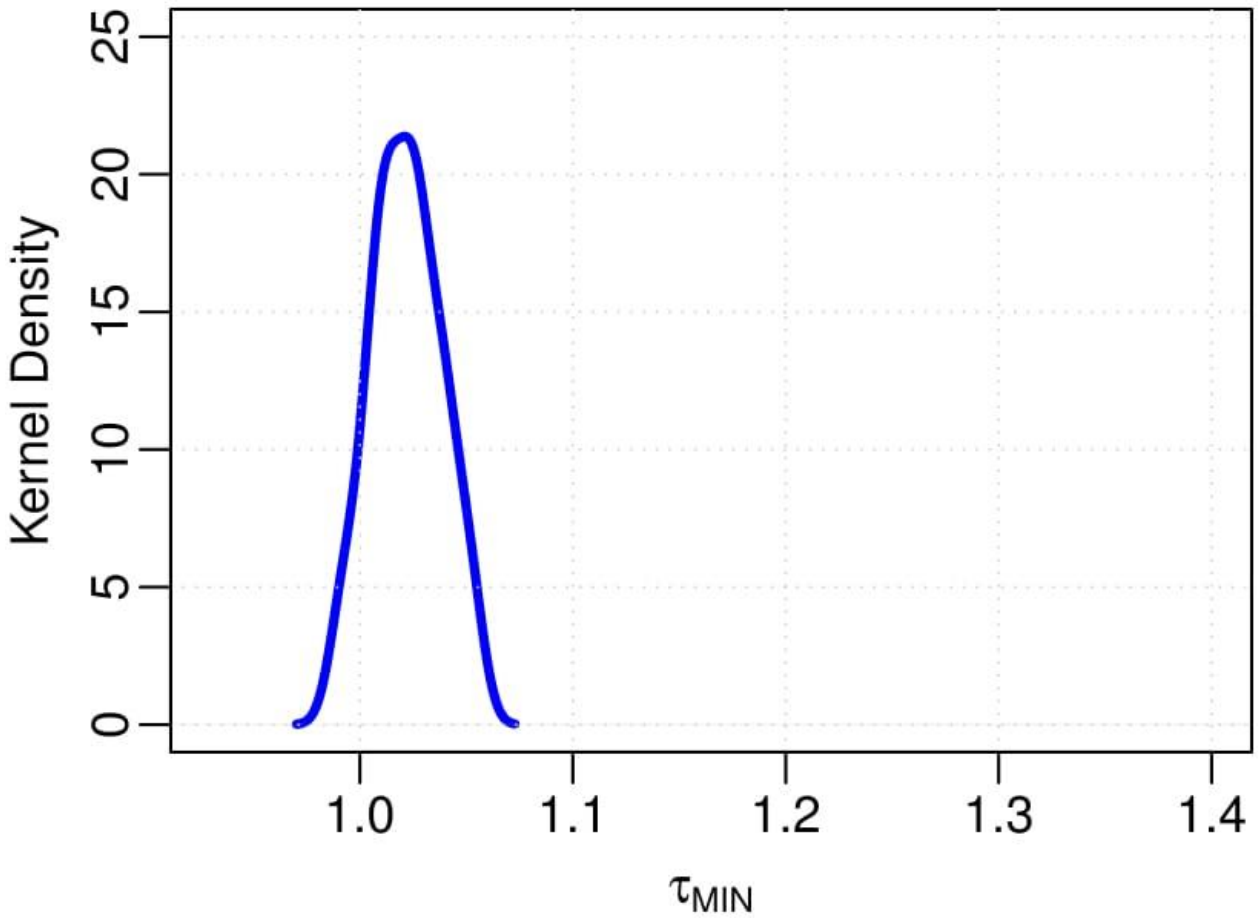
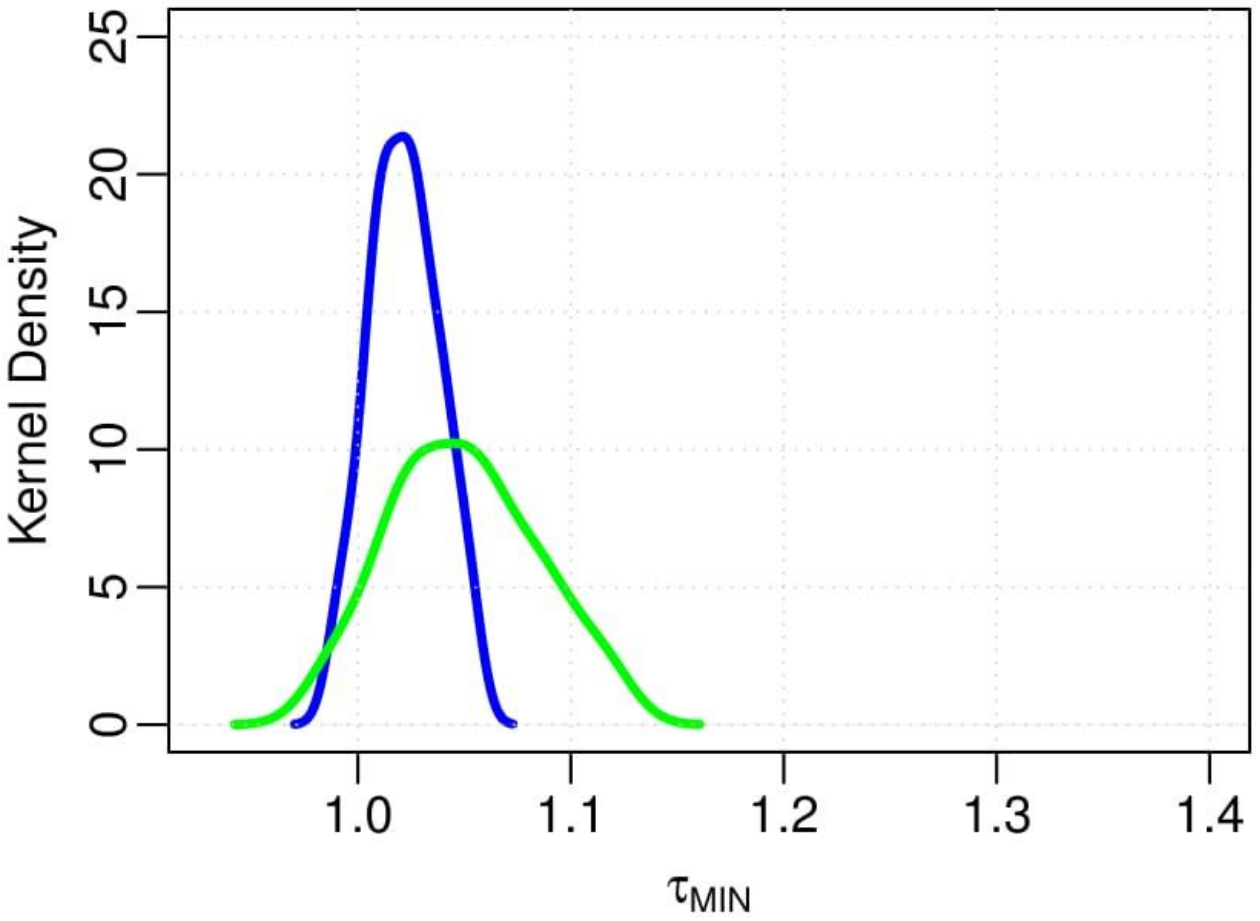


Impact on Logic Timing



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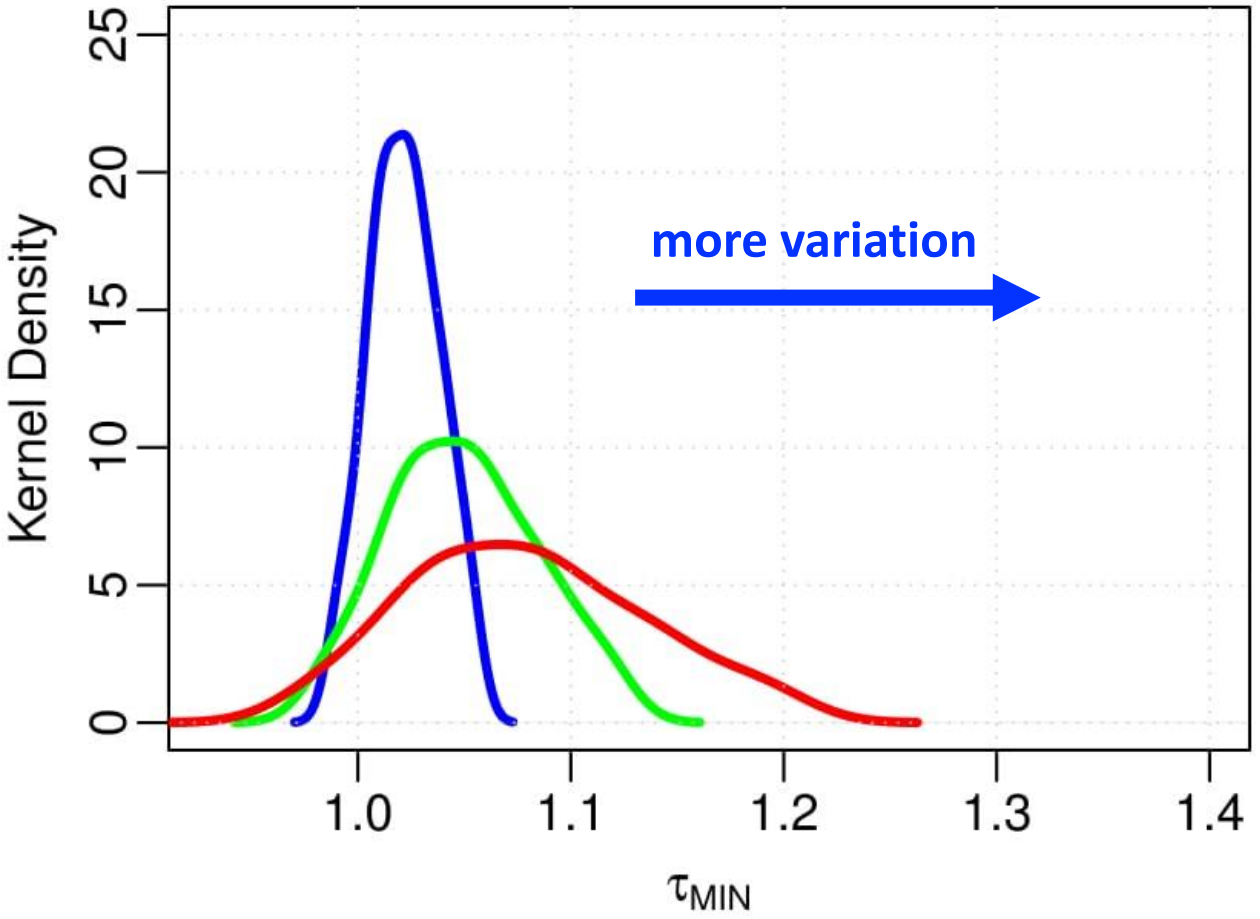

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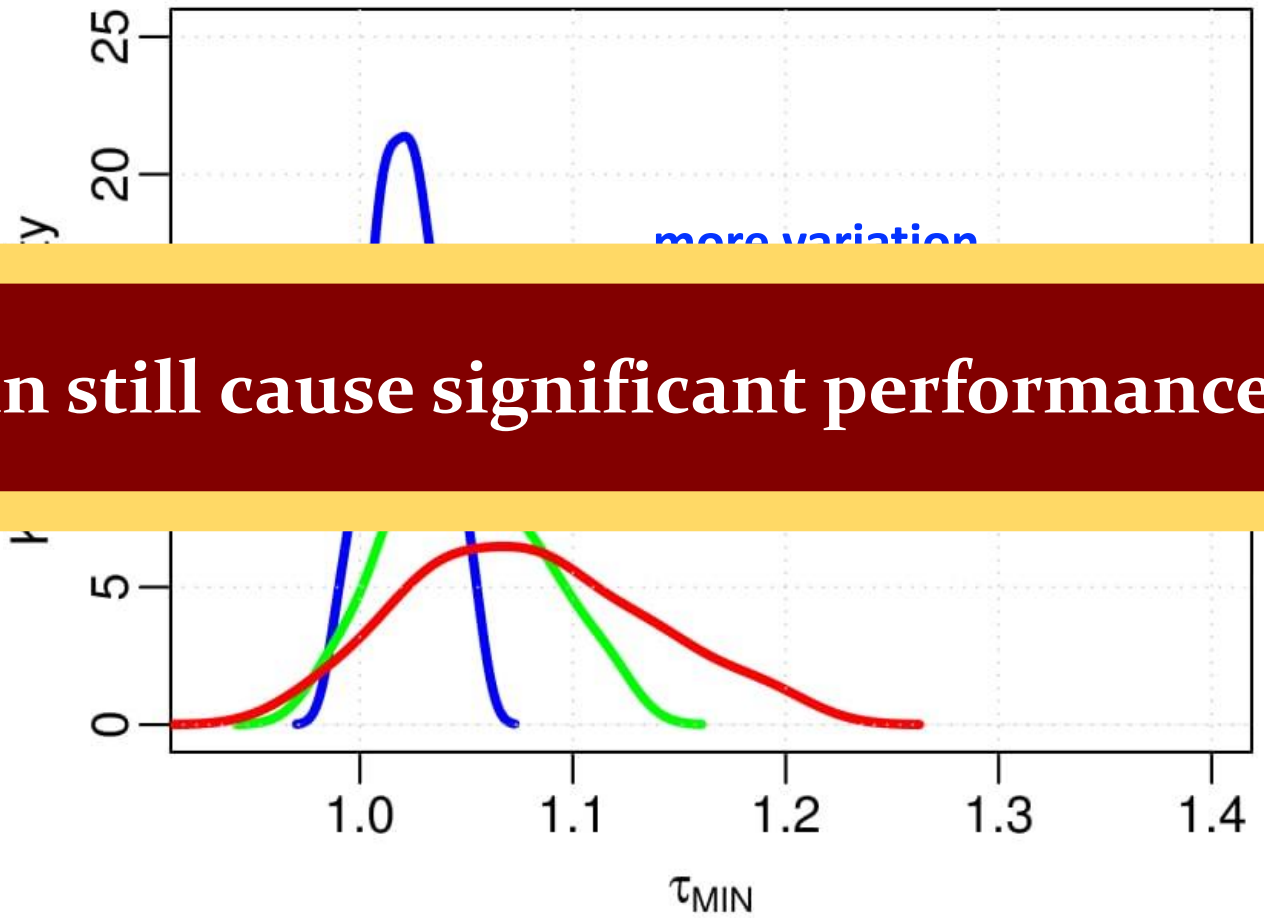

PV can still cause significant performance loss.

Impact on V_{MIN}

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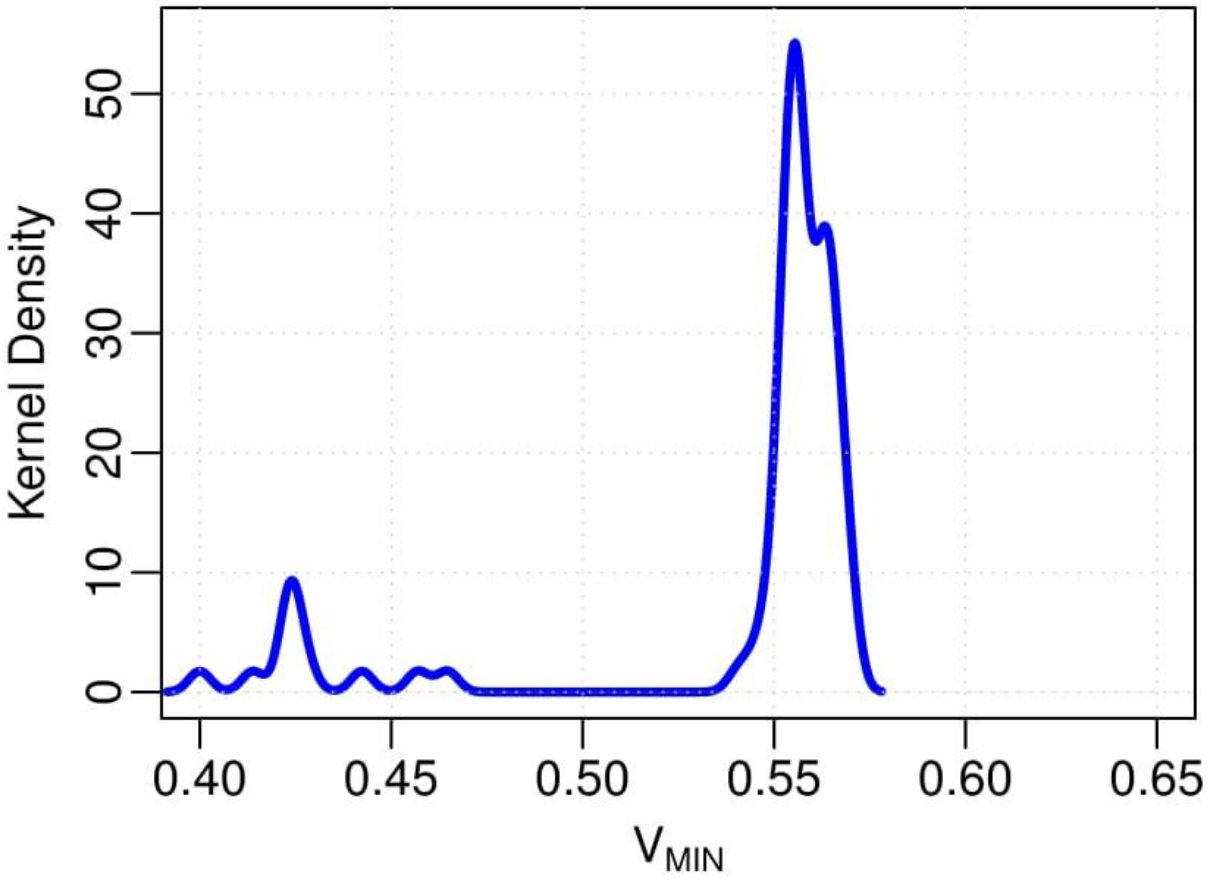

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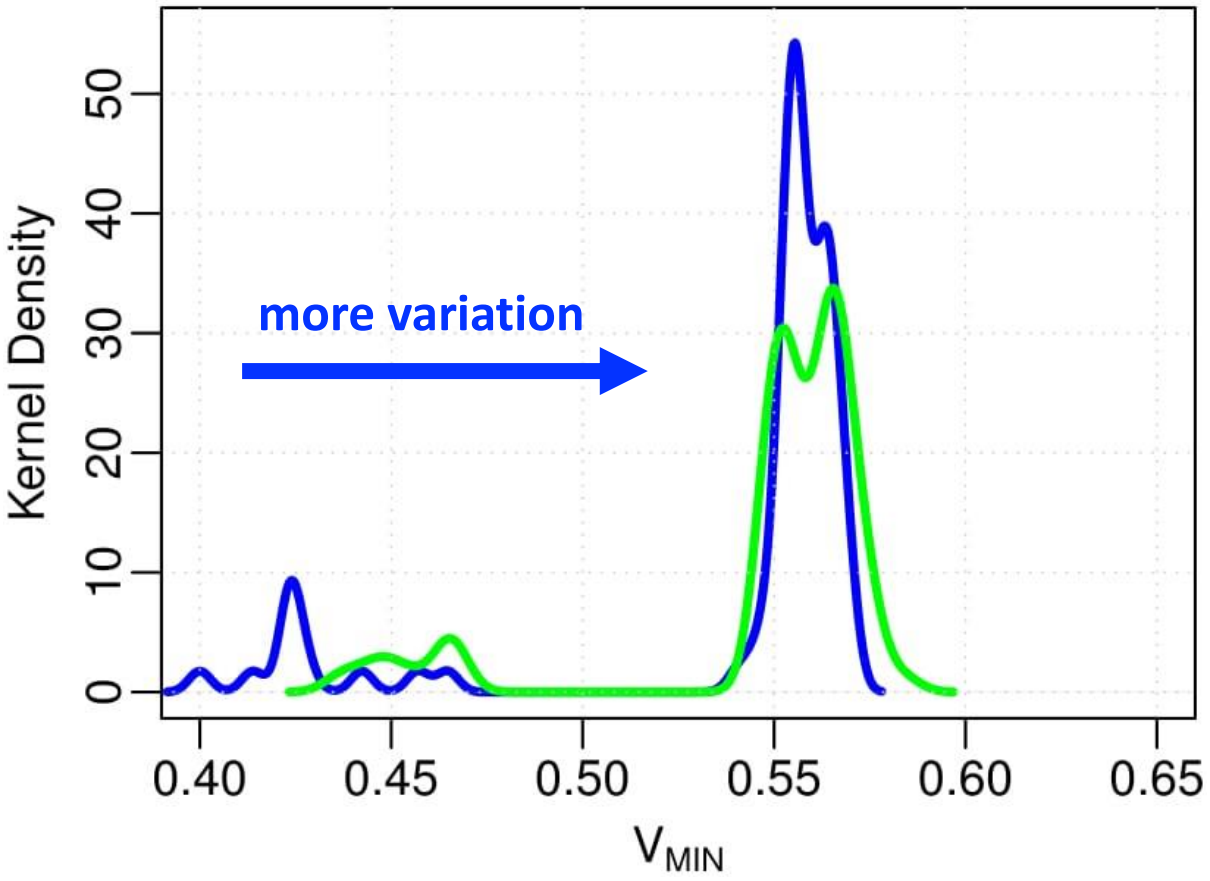
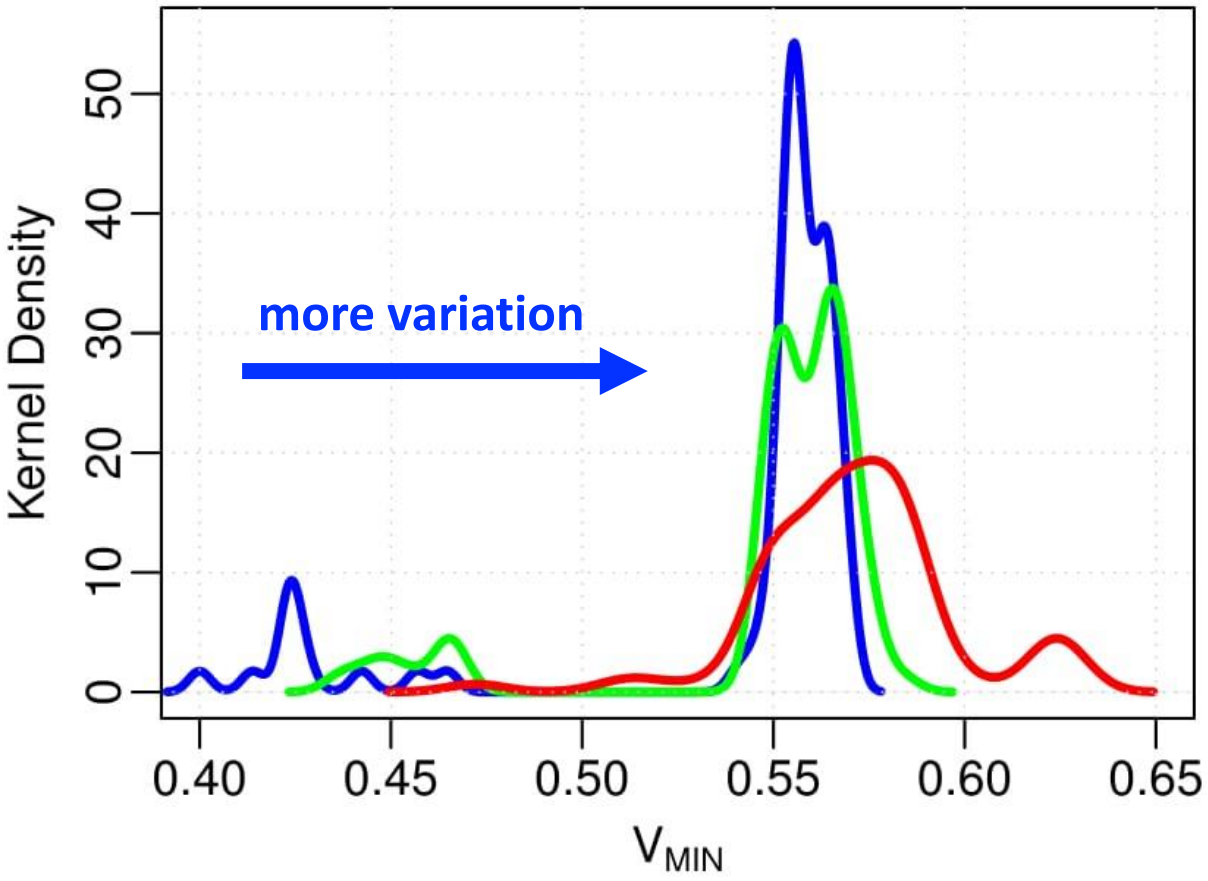
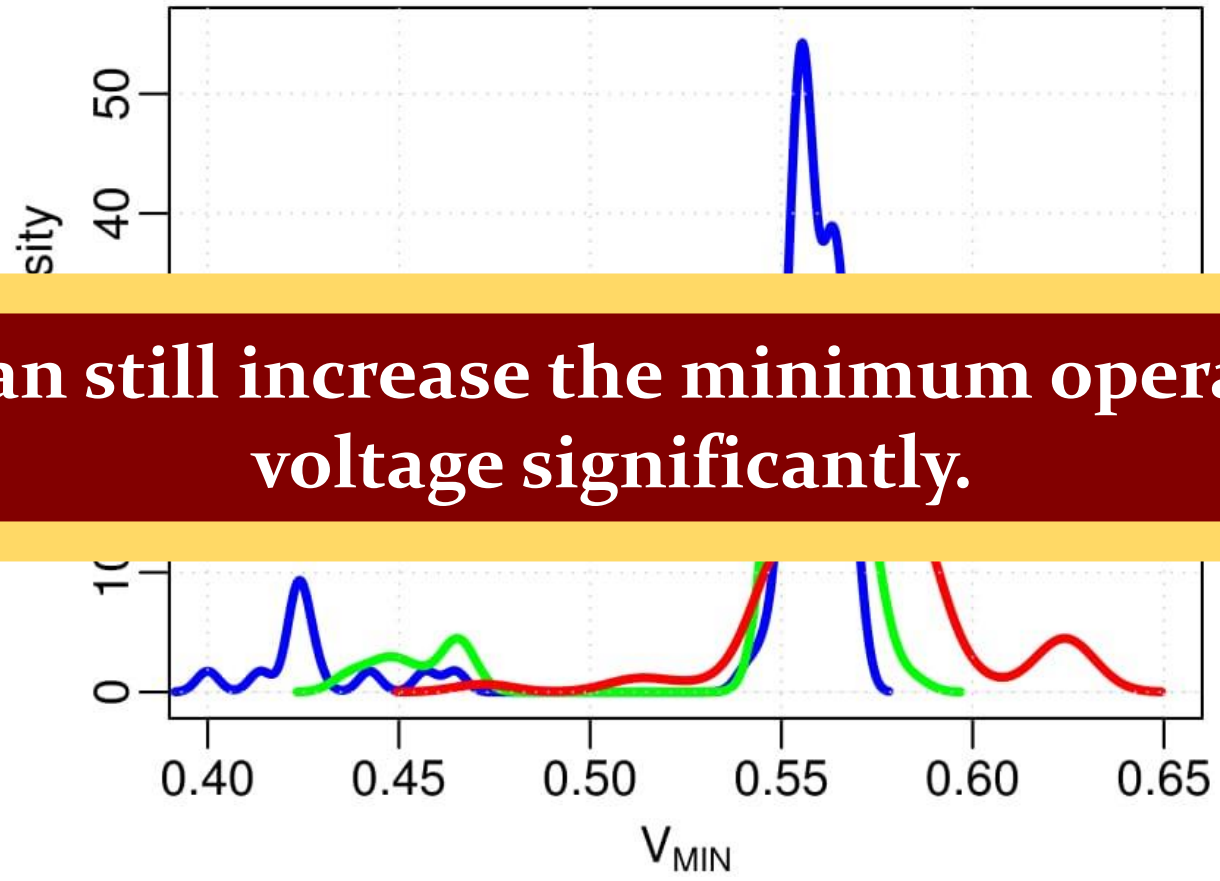


Impact on V_{MIN}



Impact on V_{MIN}



PV can still increase the minimum operating voltage significantly.

Example Use Case

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- Reducing operating voltage reduces power consumption.

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  - Frequency reduces, too.

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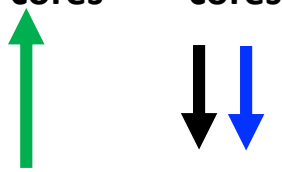

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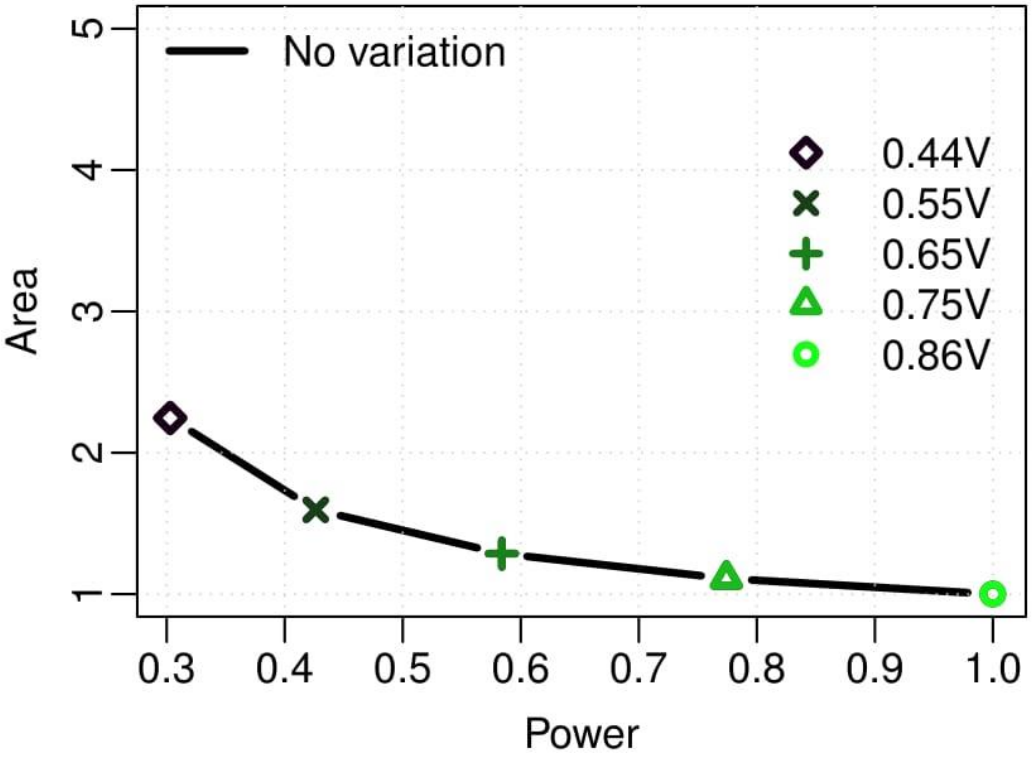

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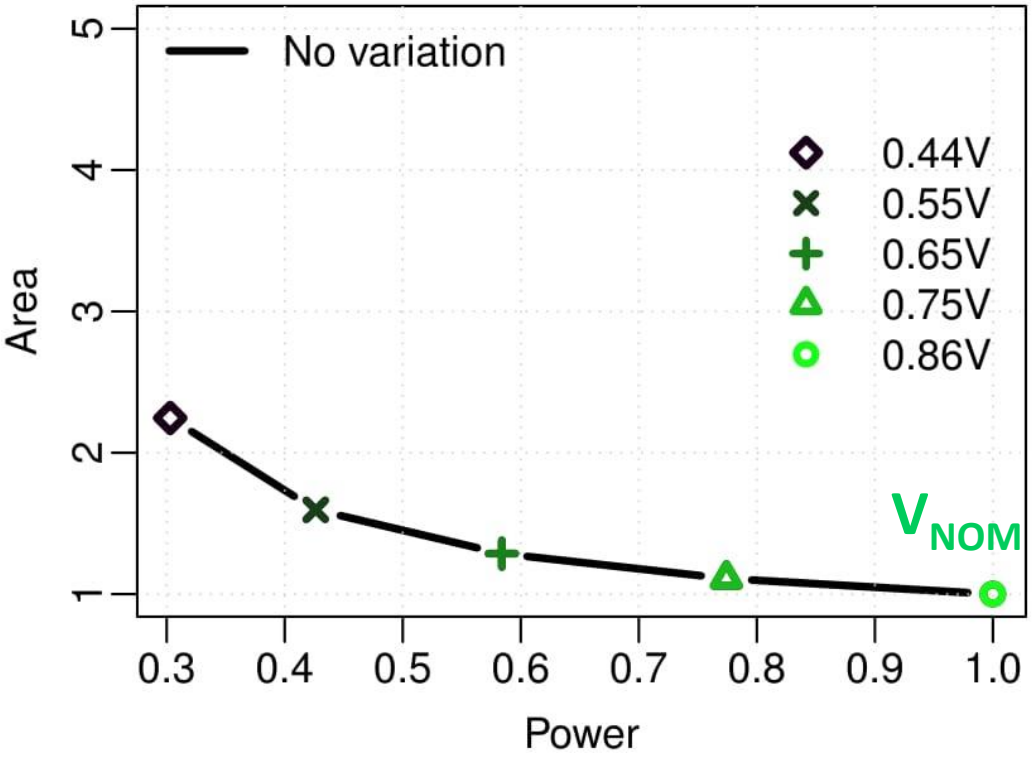

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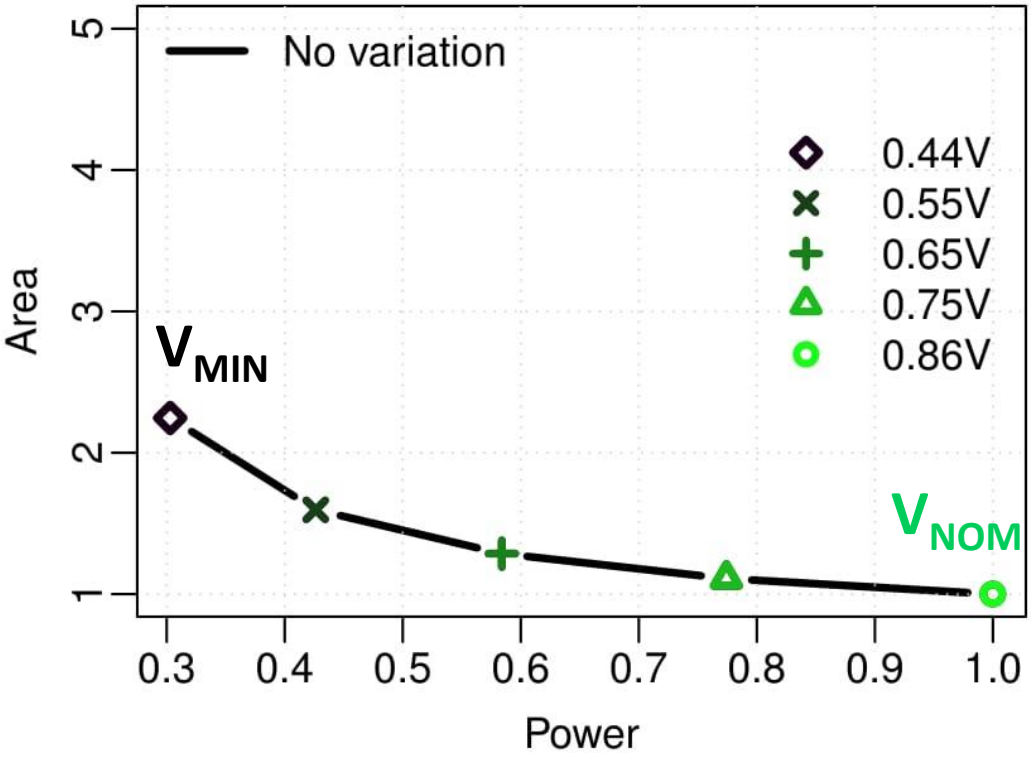

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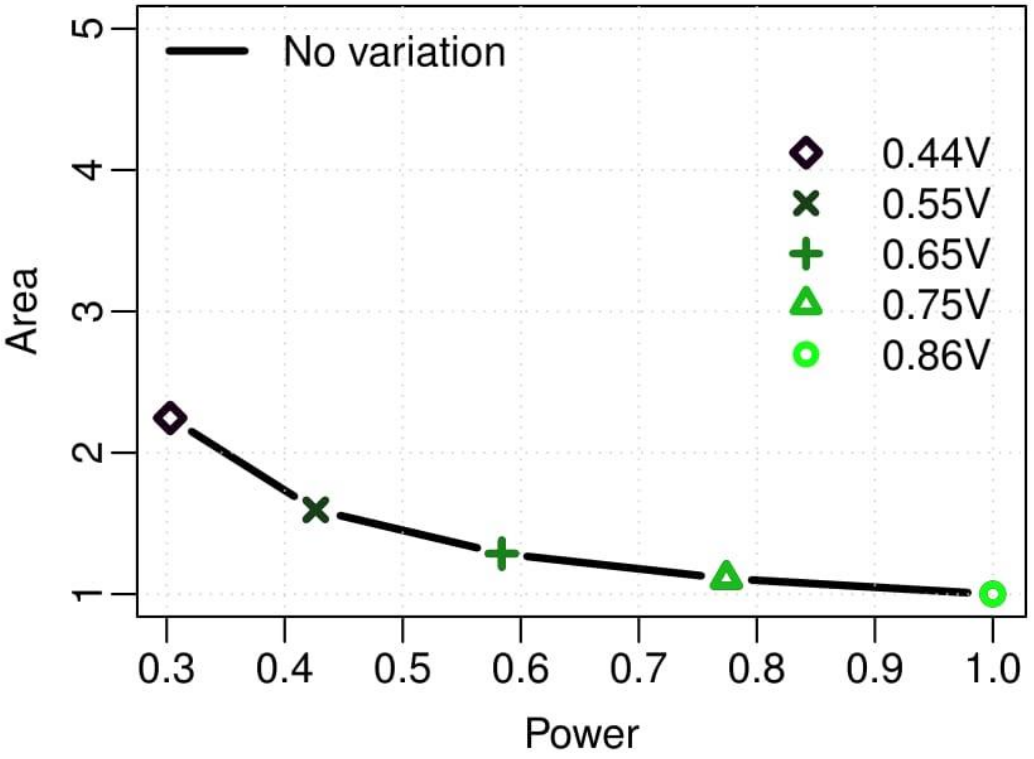

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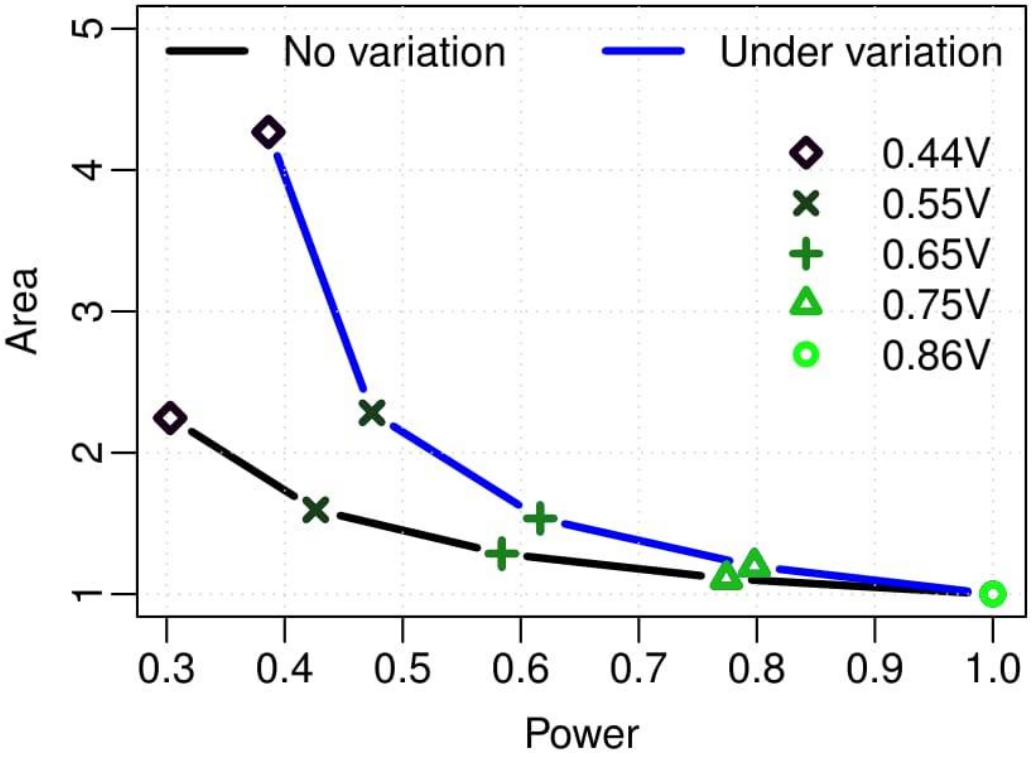

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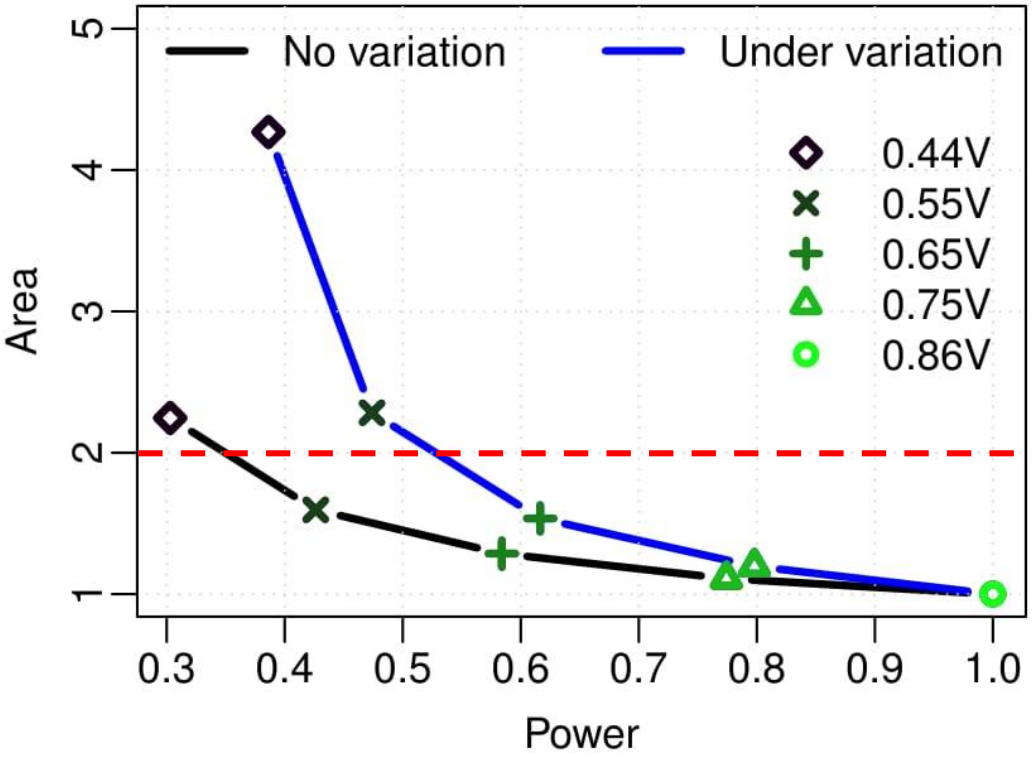

- Process Variation …
  - If > 2x area increase is not affordable…

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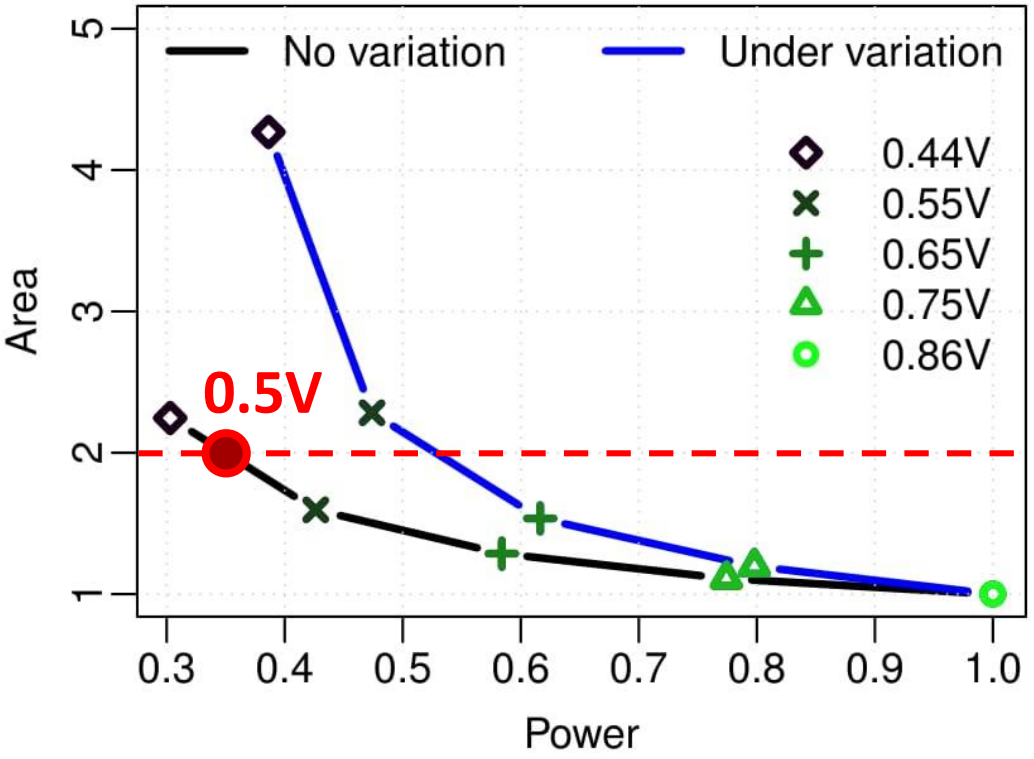

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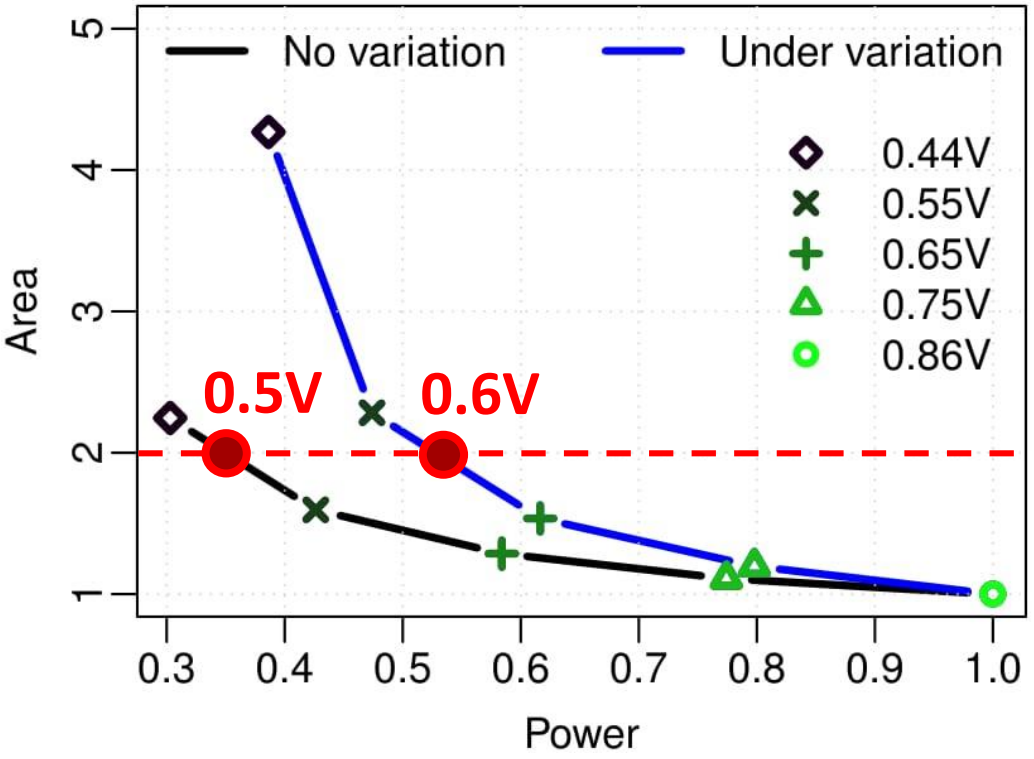
Throughput $\propto N_{cores} \times f_{cores}$



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Related Work

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- **VARIUS-TC**'s strength
  - Probabilistic model to analyze **processor logic** and **error modes of memory**

Conclusion

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- Modularity eases experimentation with different designs (e.g., SOI variants)

VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches

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