VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches

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10/5/2016
Motivation

• Manufacturing process becomes less controllable under aggressive scaling.
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  ➢ Deviation of device parameters from nominal becomes more likely.
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• **Contribution: VARIUS-TC**
  ➢ Modeling process variation in emerging devices at architecture-level.
Thin Channel (TC) devices

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Traditional Planar CMOS

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Traditional Planar CMOS

Channel Thickness

Thin Channel (TC) devices

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SOI

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FinFET

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VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches
VARIUS-TC: Overview
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VARIUS-TC: Overview

**Floorplan**

- **Device Module**
  - LUT
  - Path delay distribution
- **Circuit Module**
- **Architecture Module**

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VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches
Hierarchical Variation Modeling

Systematic variation
Hierarchical Variation Modeling

Systematic variation

- Spatial correlation
Hierarchical Variation Modeling

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Systematic variation

• Spatial correlation
• Grid granularity
Hierarchical Variation Modeling

Systematic variation
- Spatial correlation
- Grid granularity

Random variation
- Independent
- Device granularity

Systematic variation + Random variation
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Look-Up Table
Look-Up Table

LUT

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
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<tbody>
<tr>
<td>Voltages</td>
<td></td>
</tr>
<tr>
<td>Technology Parameters</td>
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### Look-Up Table

![LUT Diagram]

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Output

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• LUT vs. closed-form formula:

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- LUT vs. closed-form formula:
  - Modularity eases experimentation with different designs (e.g., SOI variants)
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- LUT vs. closed-form formula:
  - Modularity eases experimentation with different designs (e.g., SOI variants)
  - Robust closed-form formula may not always be available for emerging switches
VARIUS-TC: Overview

VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches
Logic Timing Model
Logic Timing Model
Logic Timing Model

Probability of a path with $\tau = \tau_i$ being exercised

$\tau_i$
Logic Timing Model
Logic Timing Model
Logic Timing Model

\[ \text{pdf} \]

\[ \tau \]

\[ \tau_{\text{NOM}} \]
Logic Timing Model

\[ \text{pdf} \]

\[ \tau_{\text{NOM}} \quad \tau_{\text{MIN}} \]
Logic Timing Model

VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches

τ_{NOM}  τ_{MIN}

Safe operating point
Logic Timing Model

\[ f_{\text{MAX}} = \frac{1}{\tau_{\text{MIN}}} \]

Safe operating point

\( \tau_{\text{NOM}} \) \hspace{1cm} \( \tau_{\text{MIN}} \)
Logic Timing Model

\[ \tau_{\text{MAX}} = \frac{1}{\tau_{\text{MIN}}} \]

Safe operating point
Logic Timing Model

Error probability if clocked at $\tau_{\text{NOM}}$

Safe operating point

$f_{\text{MAX}} = \frac{1}{\tau_{\text{MIN}}}$
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Memory Model
Memory Model

- Supports 6T and 8T memory cell
Memory Model

• Supports 6T and 8T memory cell
• Timing errors
  • Write timing
  • Read timing
Memory Model

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• Timing errors
  • Write timing
  • Read timing
• Stability errors
  • Hold error
  • Write Stability
Hold Error
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- The cell is not accessed.
Hold Error

- The cell is not accessed.
- Node $V_L$ looses its state.
Hold Error

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  - Excessive leakage
Hold Error

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**VARIUS-TC**

- Minimum $V_{dd}$ ($V_{MIN}$) to exclude state loss
Evaluation Setup
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- Device parameters
  - PTM, FinFET, 16nm
Evaluation Setup

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• Parametric sweep
  • $L_{\text{Fin}}$, $T_{\text{Fin}}$, $\phi_g$
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  - low, medium, high

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  - $L_{\text{Fin}}$, $T_{\text{Fin}}$, $\phi_g$

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  - low, medium, high

- Many-core system
  - 16 tiles
  - 4 core per tile
  - Private L1, Shared L2

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Impact on Logic Timing
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Planar CMOS

Kernel Density

$\tau_{\text{MIN}}$
Impact on Logic Timing

![Graph showing kernel density for FinFET and Planar CMOS](image)

- **FinFET**
- **Planar CMOS**

The graph illustrates the impact on logic timing between FinFET and Planar CMOS technologies, showing distinct kernel density distributions for each.
Impact on Logic Timing
Impact on Logic Timing

![Graph showing kernel density distribution of τ_MIN]

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- ICCD’16
- 10/5/2016
Impact on Logic Timing

more variation
Impact on Logic Timing

PV can still cause significant performance loss.
Impact on $V_{\text{MIN}}$
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Impact on $V_{\text{MIN}}$

more variation
Impact on $V_{\text{MIN}}$

![Graph showing impact on $V_{\text{MIN}}$]

The graph depicts the kernel density of $V_{\text{MIN}}$ with an arrow indicating an increase in variation. More variation is observed in the distribution.
Impact on $V_{\text{MIN}}$

PV can still increase the minimum operating voltage significantly.
Example Use Case
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- Reducing operating voltage reduces power consumption.
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Throughput vs. Power

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![Graph showing throughput and area vs. power for different voltages.]

Throughput is proportional to the number of cores ($N_{\text{cores}}$) multiplied by the frequency of the cores ($f_{\text{cores}}$). The graph illustrates the relationship between throughput, area, and power for different voltages, demonstrating the impact of process variation on performance metrics.
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![Graph showing throughput and area as functions of power for different voltage levels.](image)

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• **VARIUS-TC**’s strength
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• VARIUS-TC’s strength
  • Probabilistic model to analyze processor logic and error modes of memory
Conclusion
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- VARIUS-TC
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  • Models process variation in *emerging devices* at *architecture-level*. 
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