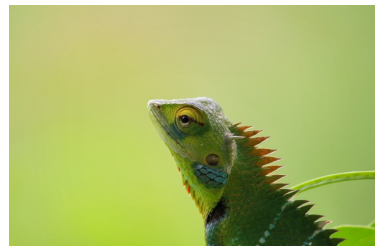


# CAMeleon: Reconfigurable B(T)CAM in Computational RAM

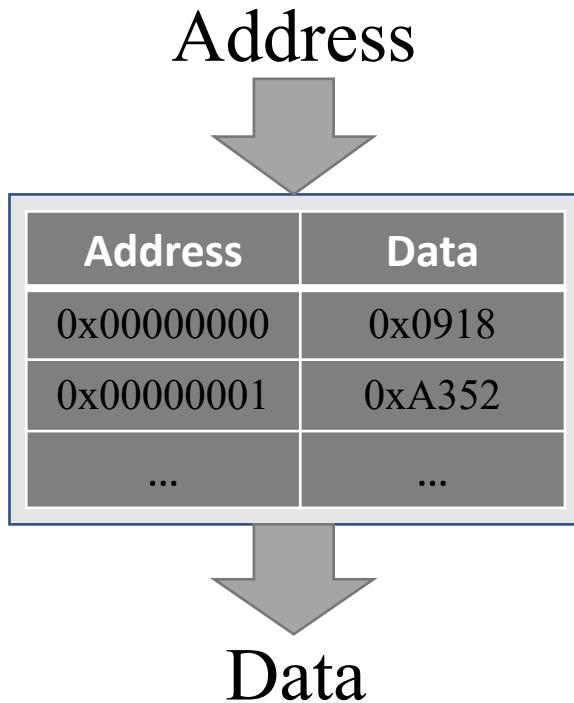
**Zamshed I. Chowdhury**, Salonik Resch, Hüsrev Cilasun,  
Zhengyang Zhao, Masoud Zabihi, Sachin S. Sapatnekar,  
Jian-Ping Wang and Ulya R. Karpuzcu

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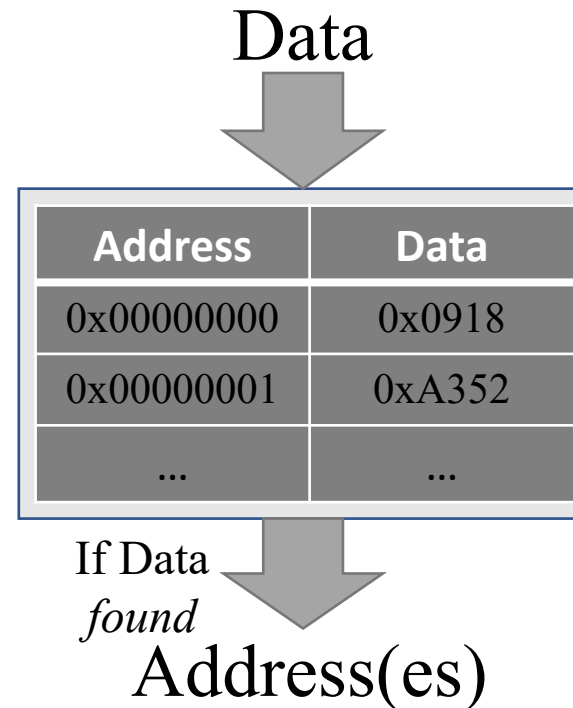
# Content Addressable Memory (CAM)

Uses SRAM, STT-MRAM, ReRAM etc.



**Conventional Memory Structure, e.g., RAM**

vs.



**Content Addressable Memory or CAM**

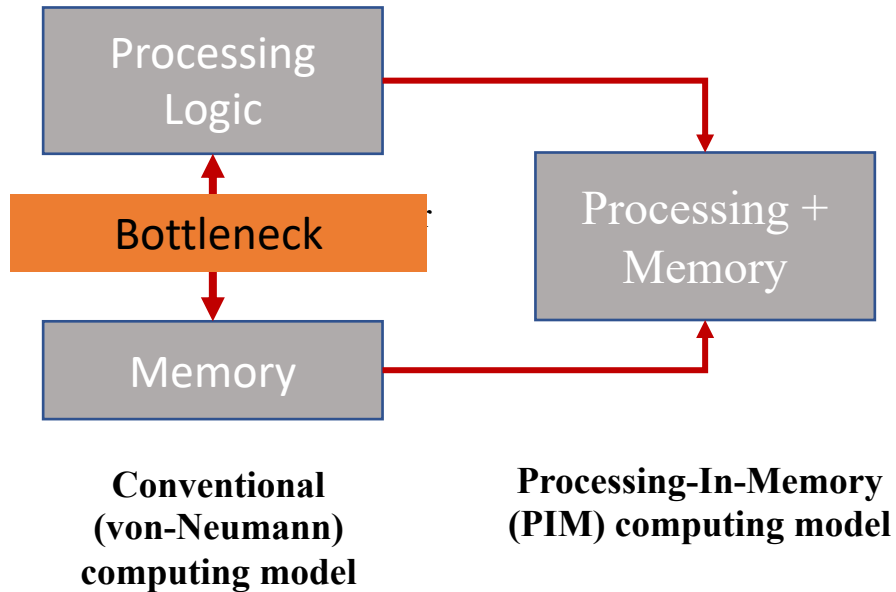
## Applications

- i. Network devices
- ii. Neuromorphic associative memory
- iii. Big-data analytics
- iv. Pattern recognition
- v. Data compression
- vi. Reconfigurable computing
- vii. Application-specific acceleration...

Edge Computing + IoT

Constrained in Area and Power budget  
Functional Reconfigurability is required

# Processing-In-Memory (PIM)



e.g., Computational RAM (CRAM)

PIM-based architectures:

- + consumes low power
- + reconfigurable between logic and memory functions



CAMeleon

- Utilizes PIM logic to implement CAM search function
- Reconfigurable between CAM and PIM
- Area and power efficient
- Comparable latency as other designs
- Scalable

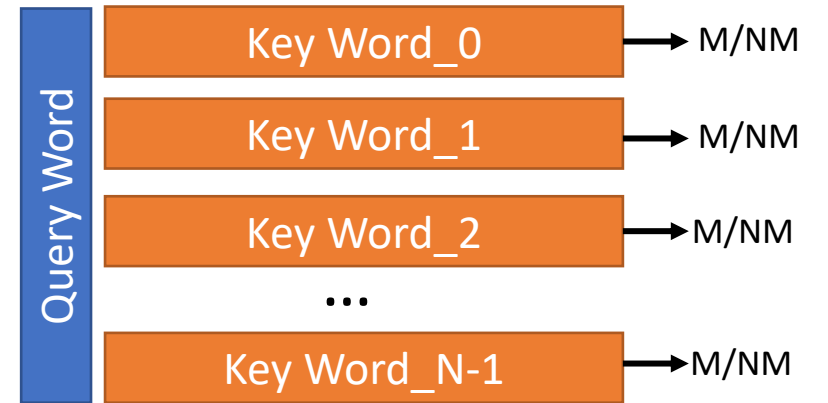
# Overview

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- Background on CAM and CRAM
- CAM Search in CRAM
- CAM and PIM modes in CRAM
- CAMeleon High-level Architecture
- Evaluation Setup and Results
- Conclusion

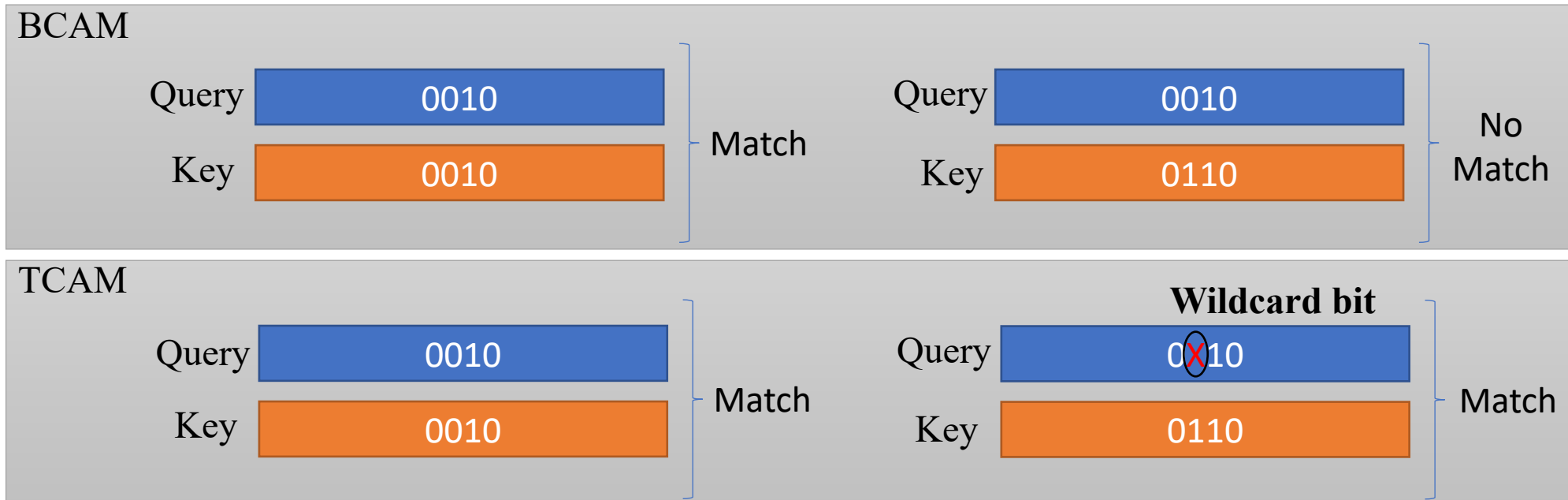
# CAM Basics

- $\text{Len}(\text{Query word}) = \text{Len}(\text{Key Word})$
- Key and Query Words are typically 32-128 bits
- Given unique key words:
  - B(inary) CAM: At most 1 match possible
  - T(ernary) CAM:  $>1$  matches possible

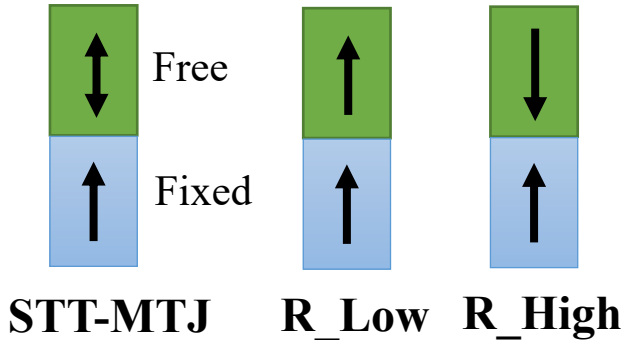


M = Match; NM = No Match

## CAM Search



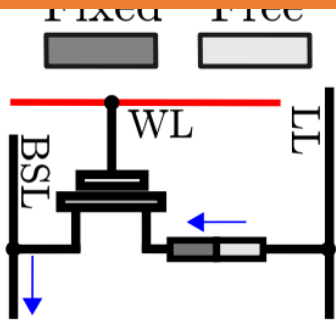
# Computational RAM (CRAM)



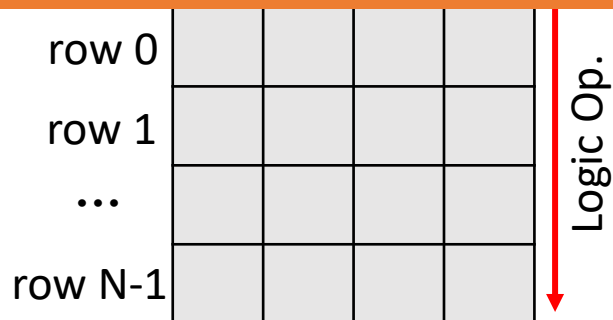
Truth Table for 2-input NOR gate

$Input_1$	$Input_2$	$Output$	$I_{OUT} = I_1 + I_2$
0 ( $R_{low}$ )	0 ( $R_{low}$ )	1	$I_{00} > I_{crit}$
0 ( $R_{low}$ )	1 ( $R_{high}$ )	0	$I_{01} < I_{crit}$
1 ( $R_{high}$ )	0 ( $R_{low}$ )	0	$I_{10} = I_{01} < I_{crit}$
1 ( $R_{high}$ )	1 ( $R_{high}$ )	0	$I_{11} < I_{crit}$

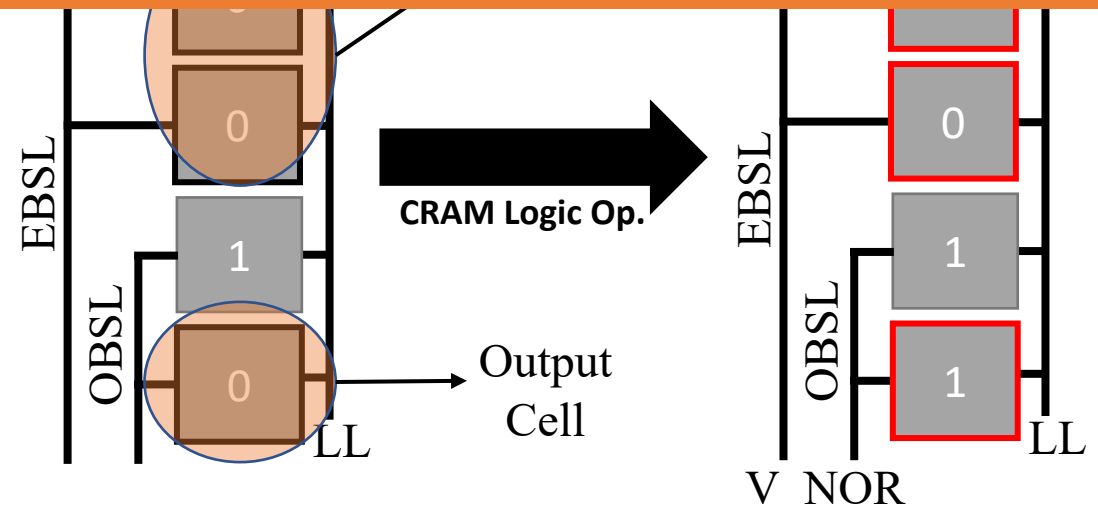
## CRAM is Boolean Complete



CRAM Cell



CRAM Tile



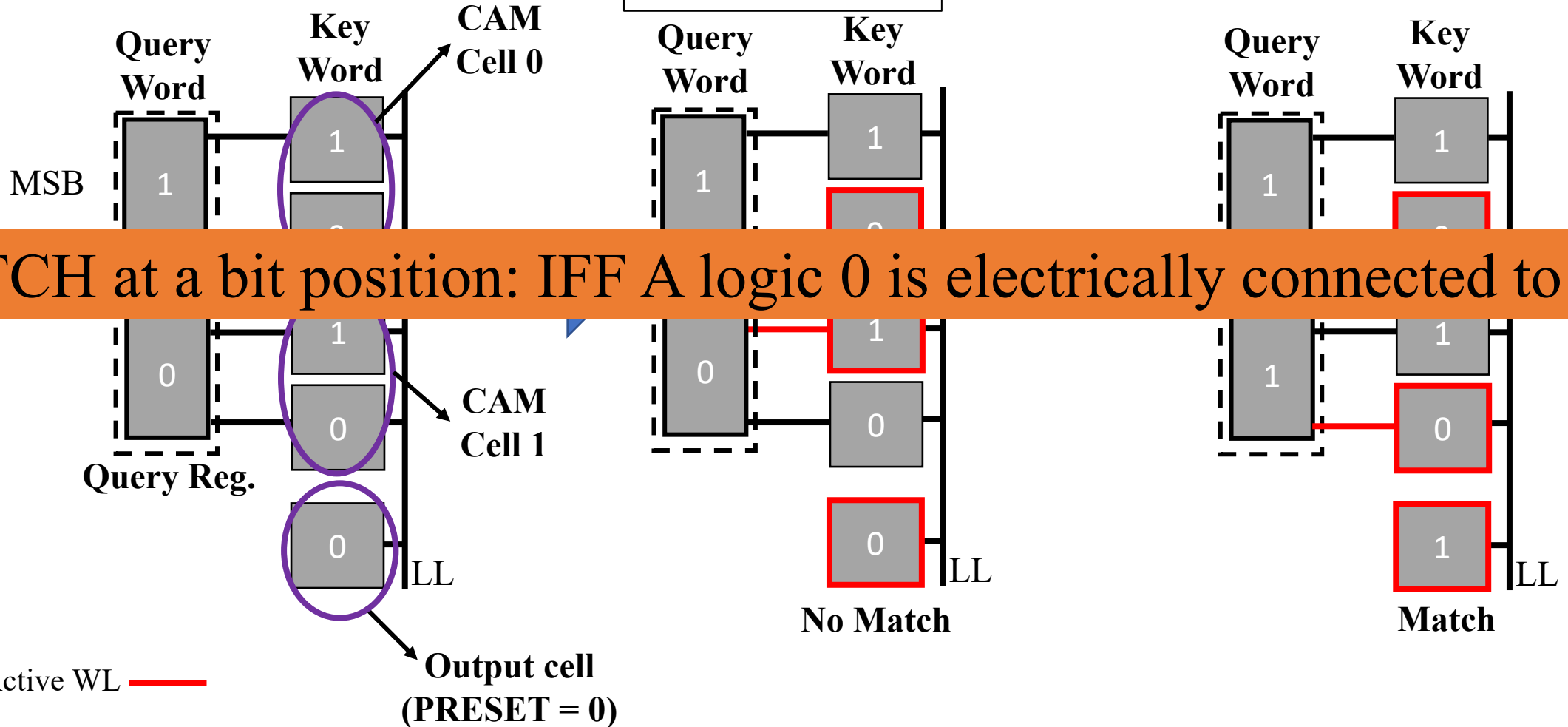
EBSL = Even Bit Select Line  
OBSL = Odd Bit Select Line

# BCAM in CRAM

<b>Key Word</b>	1	1
<b>Query Word 0</b>	1	0

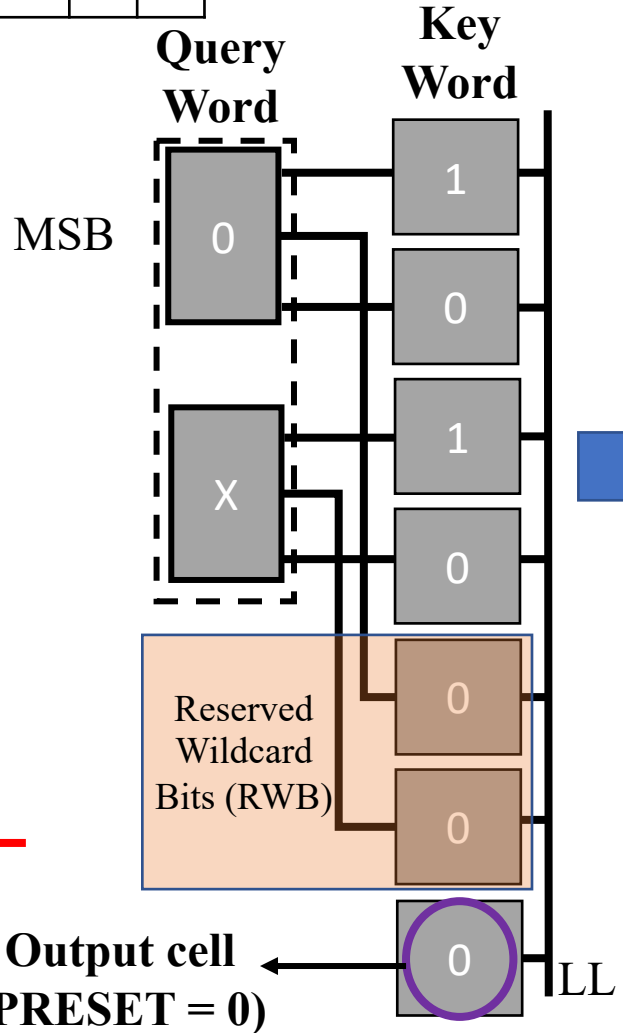
If Query bit == 0:  
Select First CAM bit  
Else:  
Select Second CAM bit

<b>Key Word</b>	1	1
<b>Query Word 1</b>	1	1



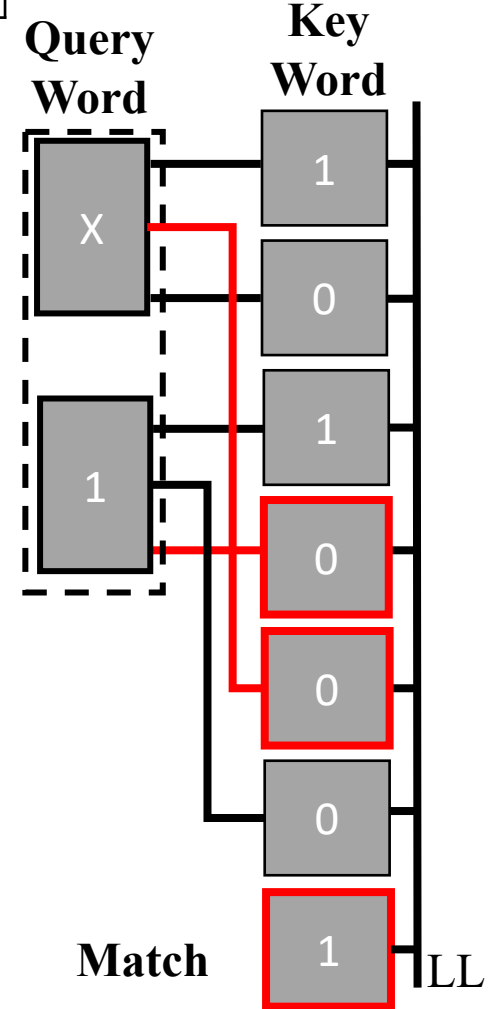
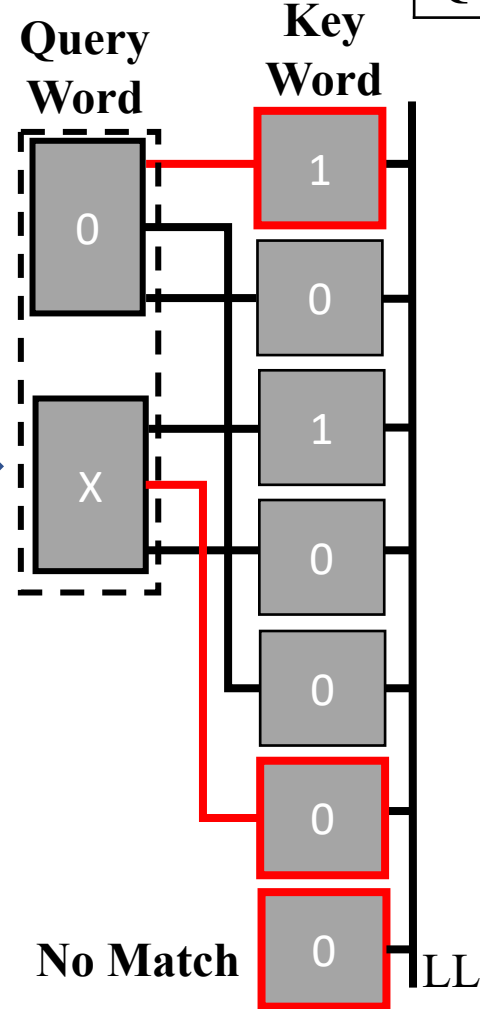
# TCAM in CRAM

<b>Key Word</b>	1	1
<b>Query Word 0</b>	0	X



NOR

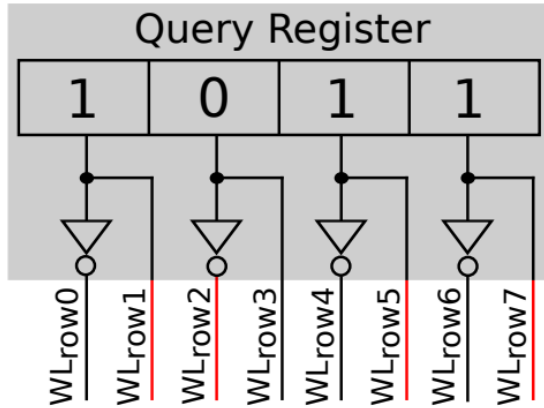
<b>Key Word</b>	1	1
<b>Query Word 1</b>	X	1



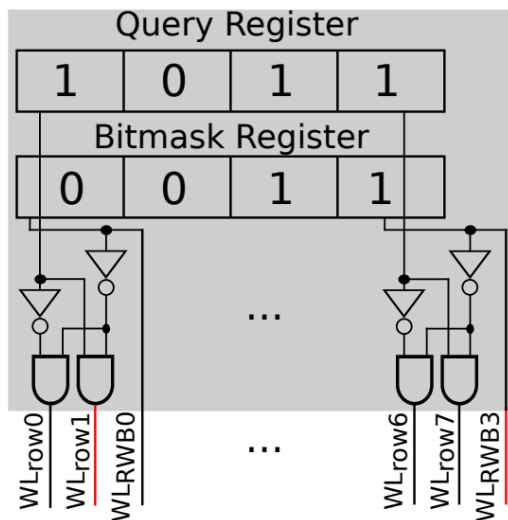


# Row Selection Logic (RSL) and CAM Mode

## RSL for BCAM



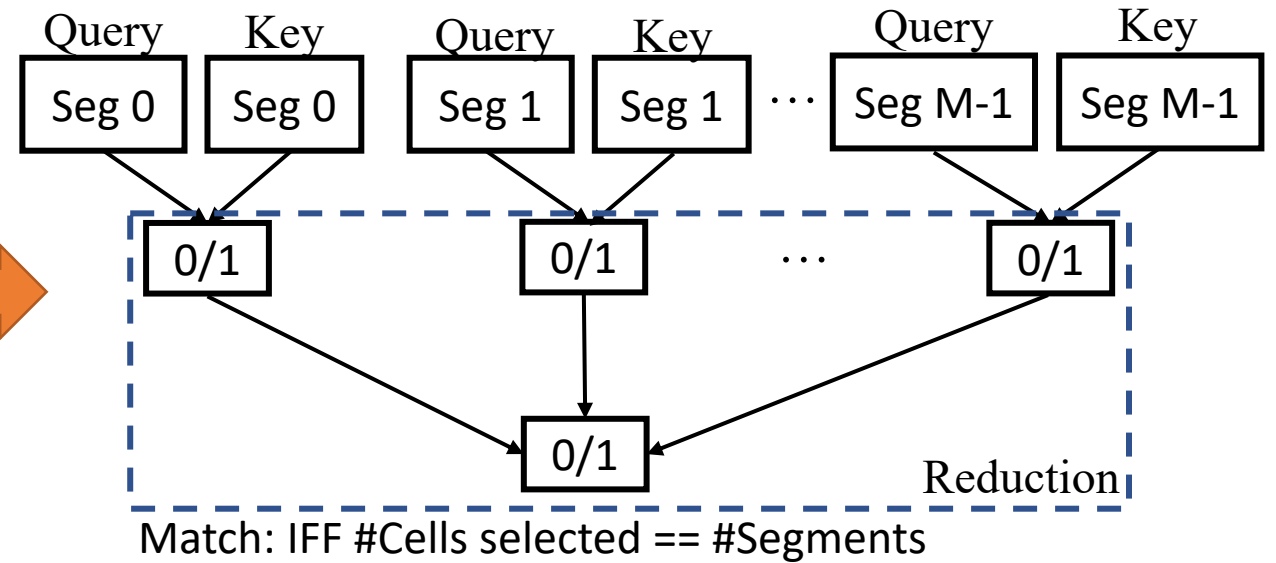
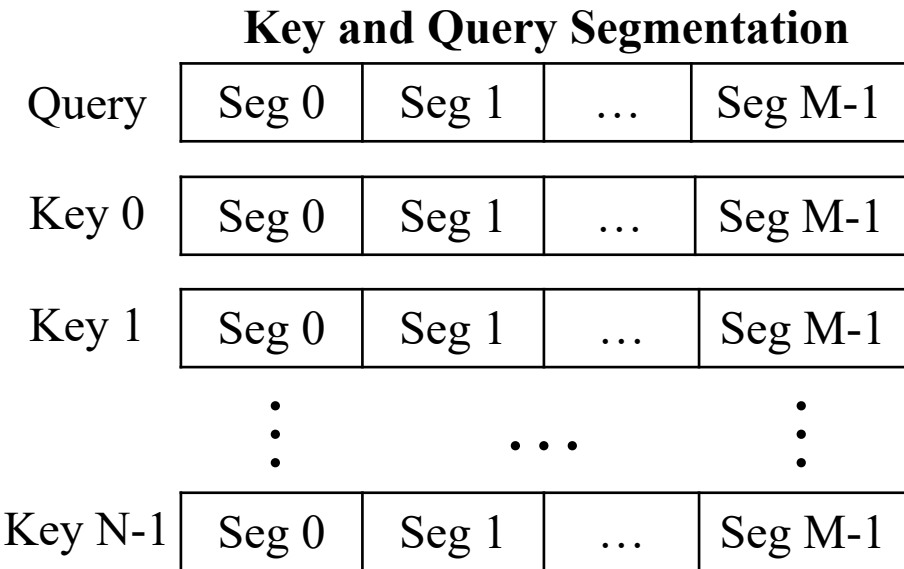
## RSL for B(T)CAM



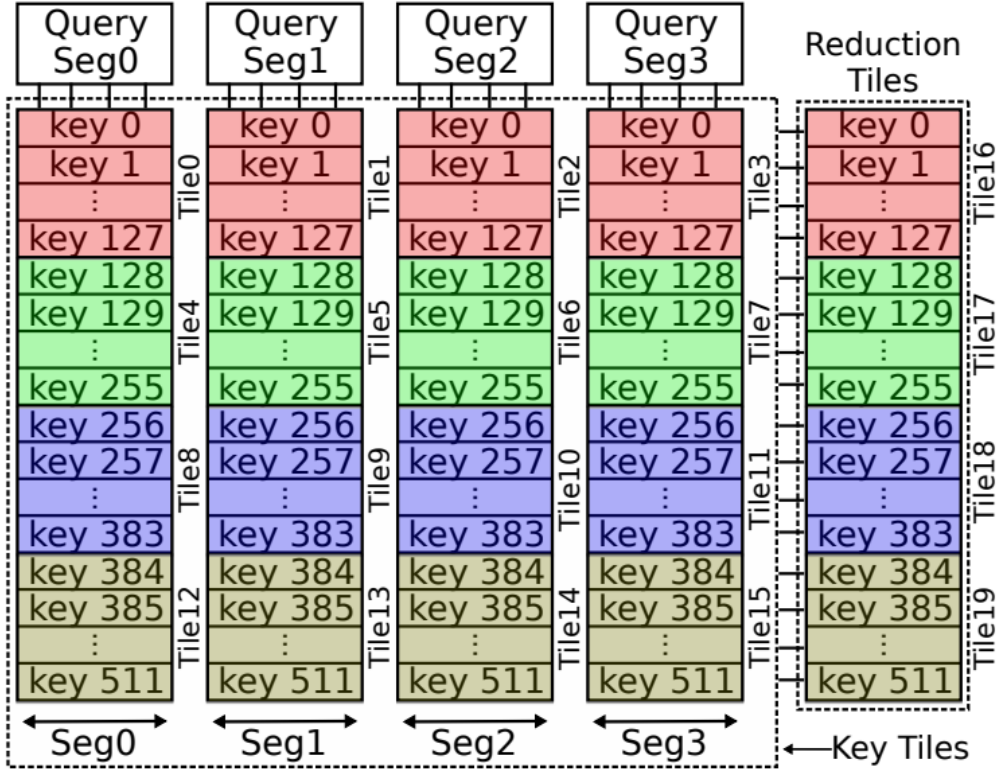
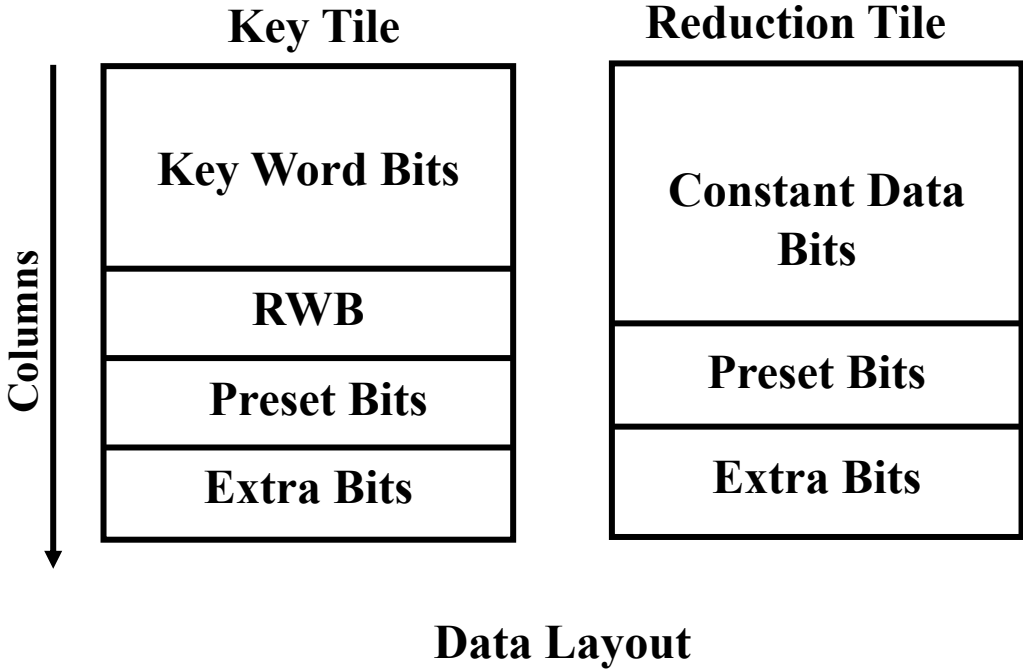
CAM Mode	Query Reg. Bit	Bit-Mask Reg. Bit	WL Signal
0	NA	NA	Tile Controller
1	1	X	RSL

**Switching between CAM and PIM modes**

# Handling Long Key and Query Words



# CAMeleon Architecture



**Organization of Tiles (transposed)**

# Evaluation Setup

Parameter	CLP	CHP	CHPA	FLP	FHP
MTJ Type	Interfacial PMTJ				
MTJ Diameter ( $nm$ )	45			10	
TMR (%)	133			500	
RA Product ( $\Omega\mu m^2$ )	5			1	
$I_{crit}$ ( $\mu A$ )	40	90	180	0.79	10
Switch. Latency ( $ns$ )	3	1	0.3	1	0.3
$R_P, R_P, R_{Trans.}$ ( $K\Omega$ )	3.15, 7.34, 1			12.7, 76.39, 1	

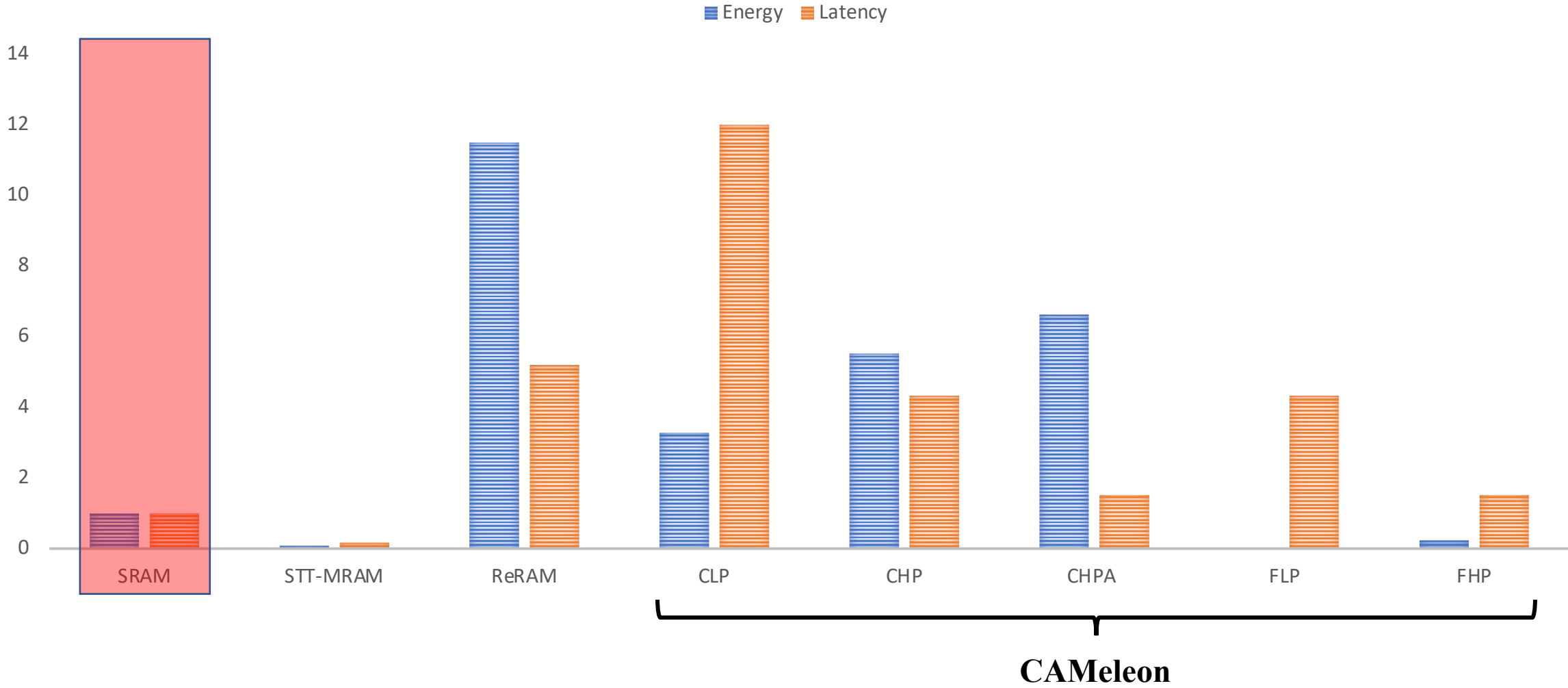
**Technology Parameters**

- \*CLP Current, Low Power MTJ
- \*CHP Current, High Performance MTJ
- \*CHPA Current, High Performance (Aggressive) MTJ
- \*FLP Future, Low Power MTJ
- \*FHP Future, High Performance MTJ

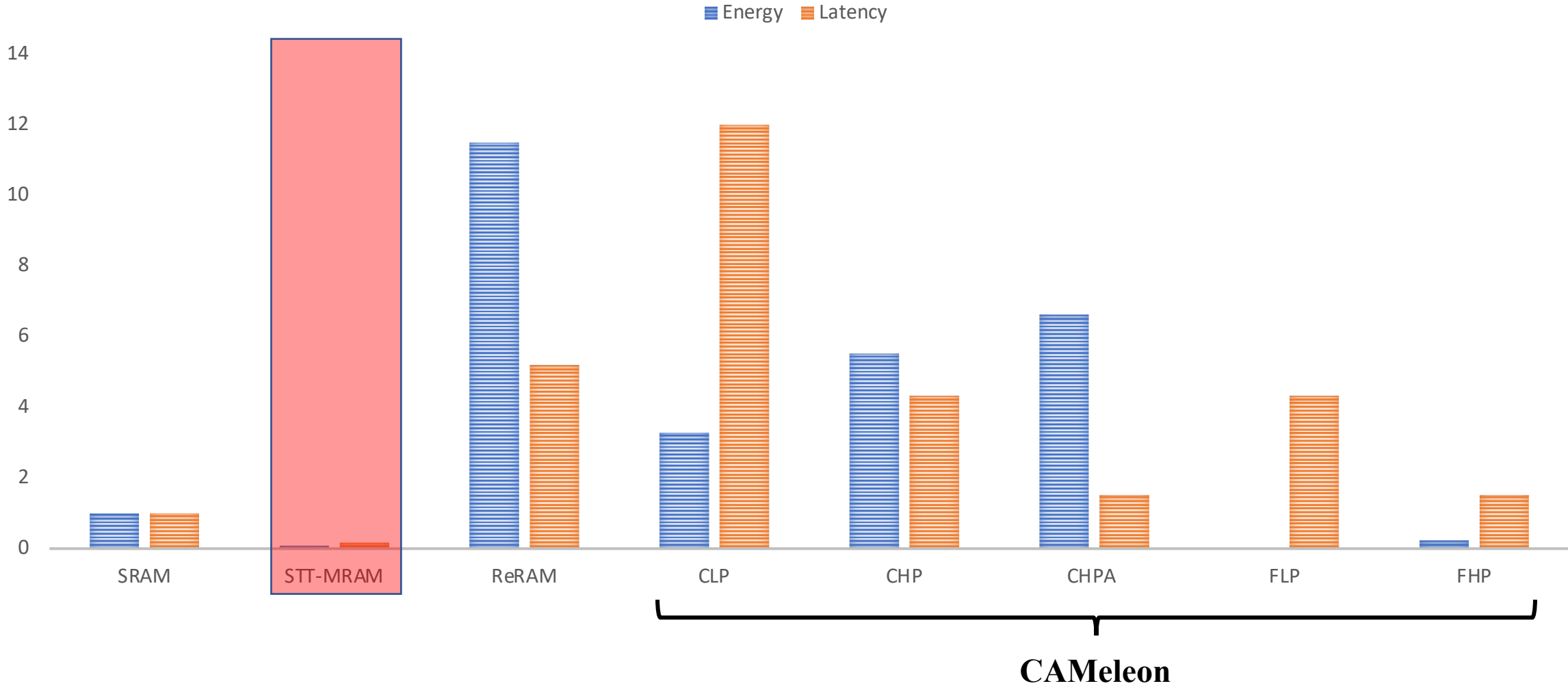
Key and Query Word Length (bits)	128
#Key Words	1024
#Query Words	102400
#Wildcard bits	64
#Segments	8

**CAMeleon Configuration**

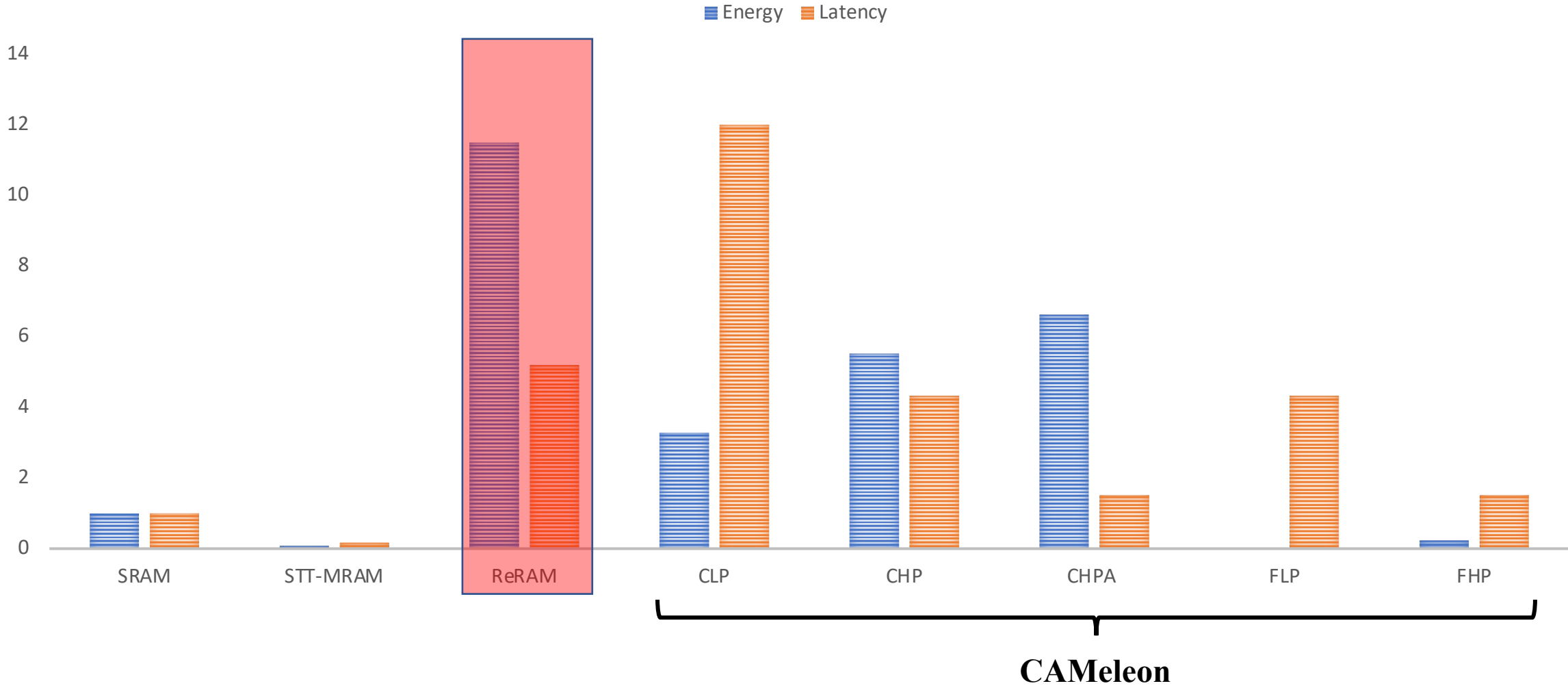
# Evaluation



# Evaluation



# Evaluation



# Evaluation

Energy Latency

14

12

CAMeleon search latency is comparable to most baselines

CAMeleon search energy is lower than most baselines

8

4

2

0

SRAM

STT-MRAM

ReRAM

CLP

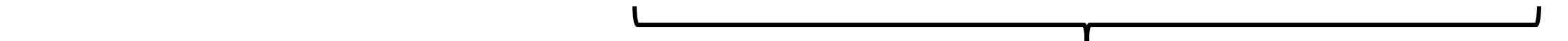
CHP

CHPA

FLP

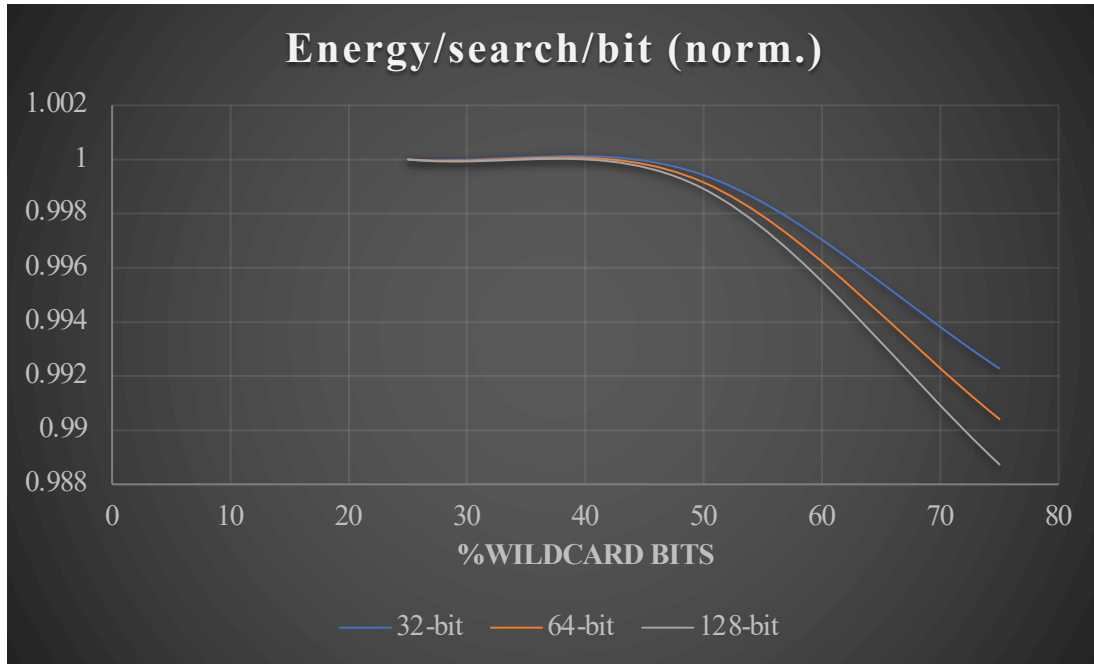
FHP

CAMeleon

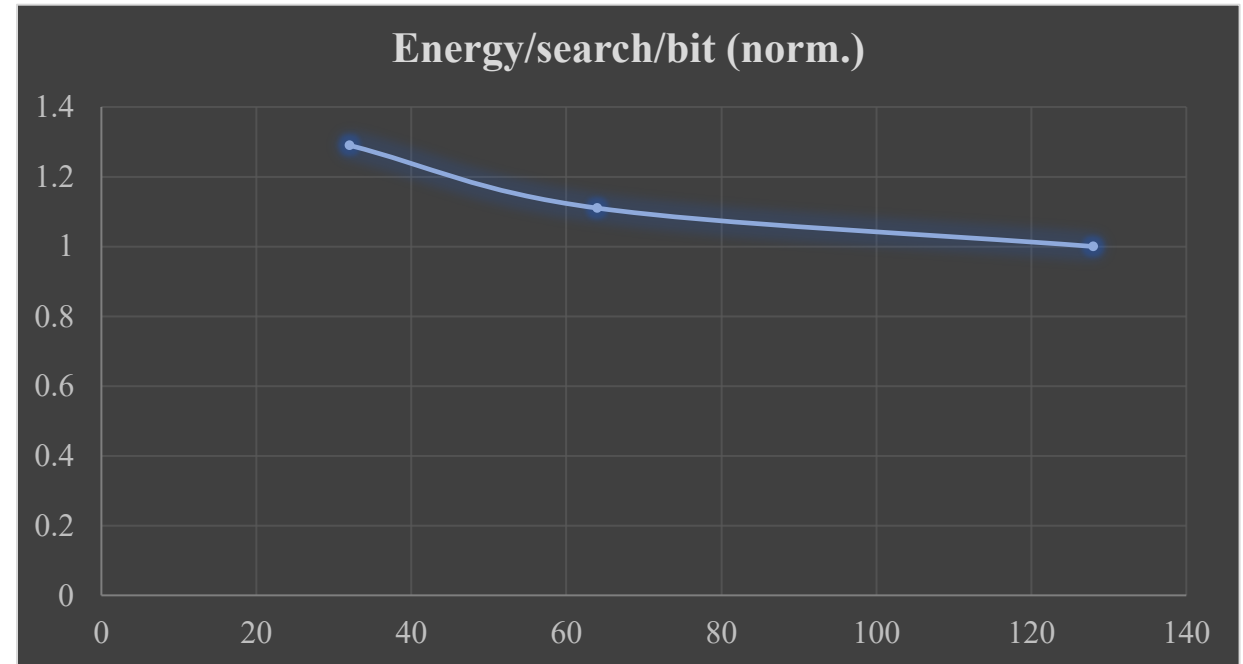




# Evaluation



**Sensitivity to %Wildcard bits in TCAM Query Word**



**Sensitivity to Query word length**

# Conclusion

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- Low overhead reconfigurability in edge and IoT systems is required
- CAMeleon: Reconfigurable between PIM and (B/T)CAM functionality
- CAMeleon outperforms a wide-range of CAM baselines, in terms of area or energy consumption (or both), while maintaining comparable search latency

Questions?