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On Gate Flip Errors in Computing-In-Memory

Zamshed I. Chowdhury, Husrev Cılasun, Salonik Resch, Masoud Zabihi, Yang Lv, Brandon Zink, Jian-Ping Wang, Sachin S. Sapatnekar, and Ulya R. Karpuzcu

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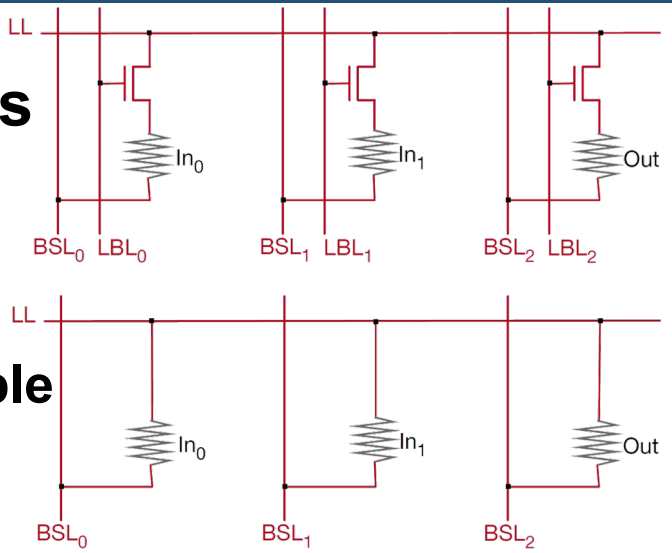
Gate Flips: A CIM-Specific Error Mode

- Computing in (nonvolatile) memory (CIM)
  - Boolean gate operations performed directly within memory
  - Great energy efficiency potential
- Functional correctness?
  - Standard models do not cover CIM-specific errors
  - Example: Gate Flips
    - Variations “flip” functionality of Boolean gates in memory
    - Each Boolean gate can behave as another

Case Study: Computing in MRAM

- **Boolean gate formation between cells**
  - **Resistive network**
  - **A voltage and a preset define each gate**
    - **Output is preset to this known value**
    - **Output switches according to truth table**
- **Example: NAND**
  - **Output is preset to 1**
  - **Output remains unchanged if inputs = 00, 01, 10**
  - **Output reset to 0 if inputs= 11**



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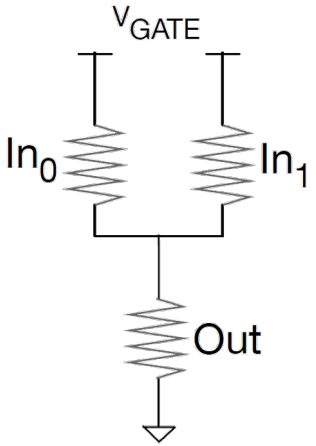
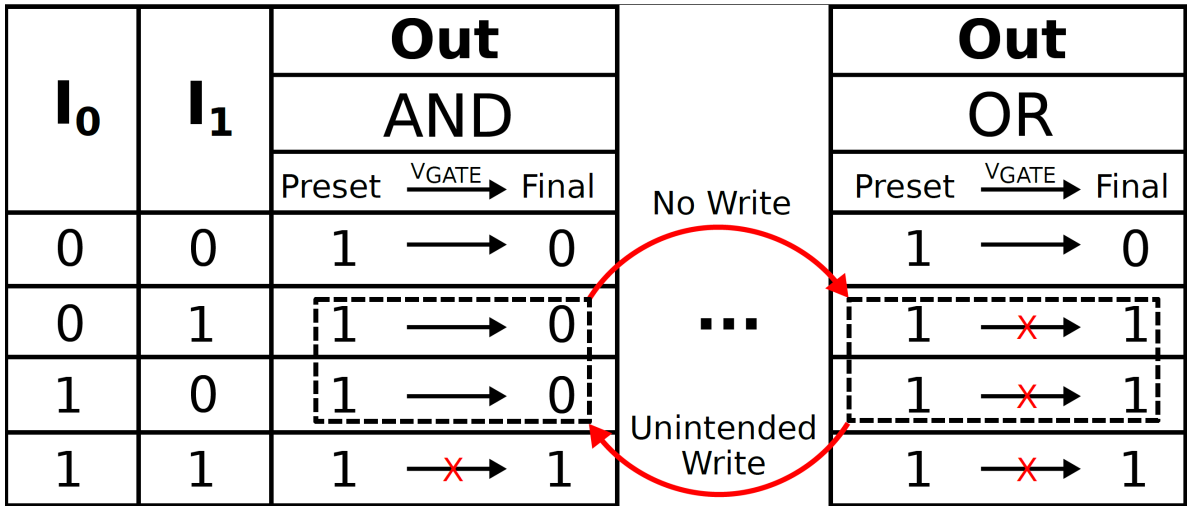


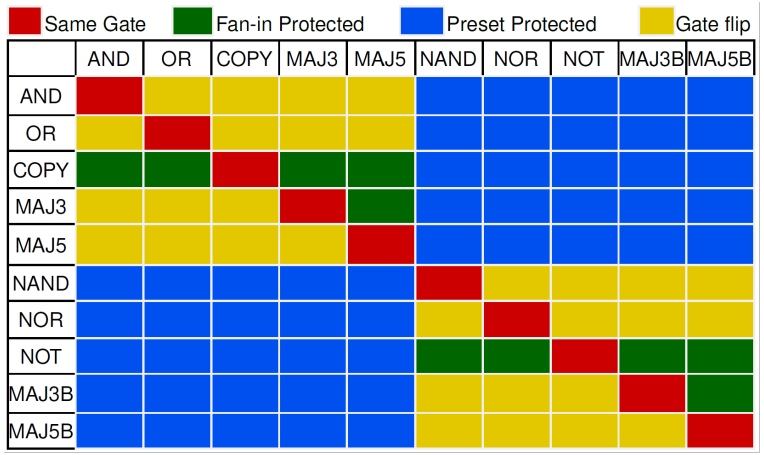
Gate Flips

- **Preset (Write) errors can cause gate flips**
  - **Preset errors: Unsuccessful or unintended writes to the output**
  - **Truth table matches a different gate**



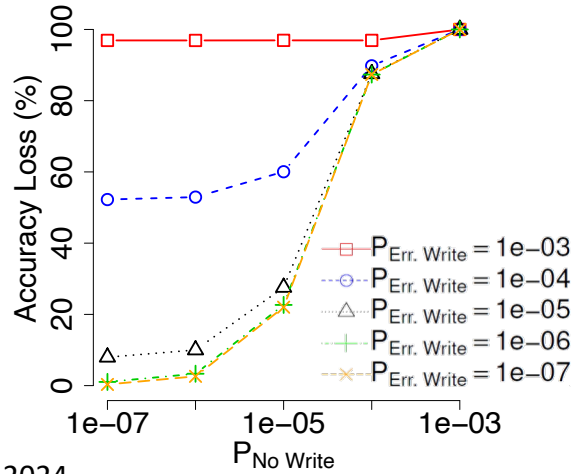
Gate Flip Matrix

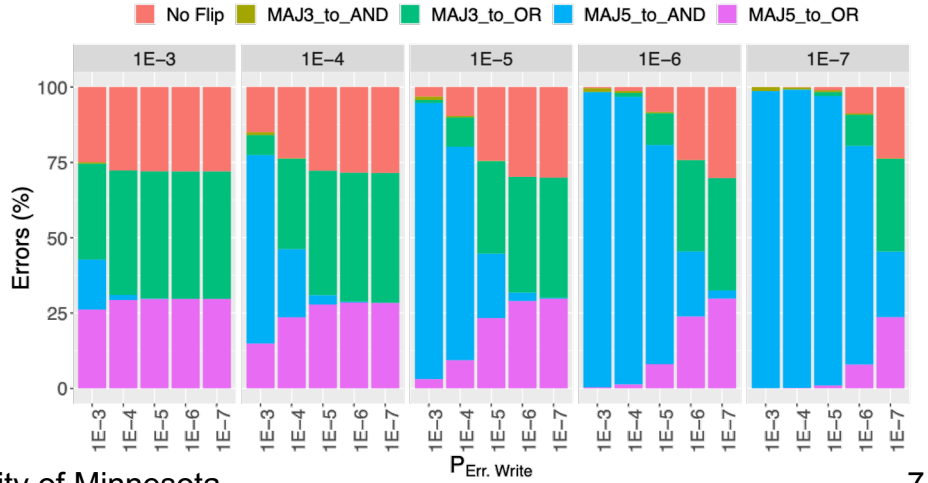
- Gate flips can be inferred from truth table
- Gate flip condition
  - Only gates of the same preset can flip to each other
  - Higher fan-in gates can flip to lower fan-in gates
    - But not vice versa
- Gate flip matrix
  - Summarizes flip patterns
  - Instrumental in
    - Functional reliability assessment
    - Forming gate libraries



Results

- **Significant portion of write errors manifest as gate flips**
  - **Statistical fault injection**
    - **Unsuccessful and unintended writes**
  - **ML, graph analytics, bioinformatics benchmarks**





Conclusion

- CIM gives rise to new error modes
  - Gate flips form one such class
- Most write errors manifest as gate flips
- High-level abstractions like the gate flip matrix can
  - Help with functional reliability assessment of CIM
  - Guide design of universal gate libraries for CIM

Thanks!

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