

EE 5364/CSCI 5204 ADVANCED COMPUTER ARCHITECTURE

FALL 2012

1 COURSE OVERVIEW

COORDINATES: M/W/F 10:10-11:00
ME 108/ME 102/UNITE
<https://moodle2.umn.edu/course/view.php?id=12127>

INSTRUCTOR:

Ulya Karpuzcu
Office: 4-155 Keller Hall
Phone: (612) 626 72 03
E-mail: ukarpuzc @ umn
Office Hours: F 16:00-18:00

TEACHING ASSISTANTS:

Sanyam Mehta	Ragavendra Natarajan
E-mail: mehta121 @ umn	E-mail: natar019 @ umn
Office: Keller Hall 6-244	Office: Keller Hall 6-244
Office Hours: Tue/F 9:00-10:00	Office Hours: M/Thu 9:00-10:00

OBJECTIVES: We are going to explore (the evolution of) basic principles of computer architecture design in detail. Subject to limitations of the underlying process technology, architectural design practices emerge in tailoring computer systems to specific application domains.

PREREQUISITES: A solid understanding of computer organization (logic design, pipelined instruction execution, memory hierarchies...) is expected. You may consult an introductory computer architecture textbook such as "Computer Organization and Design: The Hardware/Software Interface" by Hennessy/Patterson or "Structured Computer Organization" by Tanenbaum, in case necessary.

REFERENCE MATERIAL: "Computer Architecture: A Quantitative Approach", 5th Edition represents the main textbook. A collection of classical research papers can be found in "Readings in Computer Architecture" by Hill, Jouppi, and Sohi. We are going to provide a selection of related research papers for each lecture on the course website.

PROJECT: The most significant component of the EE 5364/CSCI 5204. We expect a small-scale research project. We encourage novelty, but you can also try to re-generate the results of an already published research paper. We will post a pool of ideas on the course website in addition.

EXAMS: There will be two exams, both open book/notes/... The first exam, a take-home midterm will be out on October 22 at 10:10am, and will be due October 24 by 10:10am (in class). The second exam, the final, will be held on December 18 between 8am-10am.

HOMEWORKS: There will be 4 homeworks. Each homework will cover at least one research paper. Some will demand simulation.

TOOLS: You will need an (μ -)architectural simulator for homeworks and the project. As an example simulator, we have SimpleScalar available in CSE Labs. However, you are not restricted to use SimpleScalar; the vast majority of (μ -)architectural simulators are open-source.

GRADING:	Project	35%
	Midterm	20%
	Final	30%
	Homeworks	15%

MECHANICS:

- You are **expected** to work in groups of 3-4 for homeworks and the project, modulo the UNITE students. Groups should be formed (and TAs should be notified) before the first homework gets out.
- **Due to the exceptionally large size of the class, we cannot be flexible with submission/exam dates.**
- Any non-submitted item will be processed with a grade of 0.
- If the students fail to submit at least 3 of the homeworks, their project will not be graded – practically, this will translate to a 0-grade project.
- If the students fail to take both of the exams, their project will not be graded – practically, this will translate to a 0-grade project.

2 SYLLABUS

Week	Mon	Wed	Fri	Note
1	Labor Day	Introduction	Fundamentals	
2	Fundamentals	Instruction Level Parallelism (ILP) in Hardware (HW)	ILP in HW	
3	ILP in HW	ILP in HW	ILP in HW	HW1 out: Fri
4	ILP in HW	ILP in HW	ILP in Software (SW)	
5	ILP in SW	ILP in SW	ILP in SW	HW1 due: Fri
6	ILP in SW	ILP in SW	Memory Hierarchy Design	HW2 out: Fri
7	Memory Hierarchy Design	Memory Hierarchy Design	Memory Hierarchy Design	
8	Midterm	Memory Hierarchy Design	Memory Hierarchy Design	HW2 due: Fri
9	Memory Hierarchy Design	Thread-level parallelism	Thread-level parallelism	Project proposal due: Mon
10	Thread-level parallelism	Thread-level parallelism	Thread-level parallelism	HW3 out: Fri
11	Thread-level parallelism	Thread-level parallelism	Data-level parallelism	
12	Data-level parallelism	Data-level parallelism	Thanksgiving	HW3 due: Fri
13	Data-level parallelism	Request-level parallelism	Request-level parallelism	HW4 out: Fri Project status reports due: Mon
14	Request-level parallelism	Storage Systems	Storage Systems	
15	Storage Systems			HW4 due: Mon Project reports due: Wed