EE 5364/CSCI 5204

ADVANCED COMPUTER ARCHITECTURE [3 CREDITS]

FALL 2015

1 COURSE OVERVIEW

COORDINATES: M/W 13:00-14:15
MechE 108 & UNITE
https://ay15.moodle.umn.edu/course/view.php?id=5125

INSTRUCTOR:

Ulya Karpuzcu
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Office Hours: Wed 15:00-16:00

TEACHING ASSISTANT:

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OBJECTIVES: We are going to cover explore (the evolution of) basic principles of computer architecture design in detail. Subject to limitations of the underlying process technology, architectural design practices emerge in tailoring computer systems to specific application domains.

PREREQUISITES: EE 4363/CSci 4204 or equivalent.
A solid understanding of computer organization (logic design, pipelined instruction execution, memory hierarchies...) is expected. You may consult an introductory computer architecture textbook such as Computer Organization and Design: The Hardware/Software Interface by Hennessy & Patterson or Structured Computer Organization by Tanenbaum, in case necessary.

REFERENCE MATERIAL: "Computer Architecture: A Quantitative Approach", 5^{th} Edition represents the main textbook. "Modern Processor Design" by Shen & Lipasti is recommended. A collection of classical research papers can be found in "Readings in Computer Architecture" by Hill, Jouppi, and Sohi. We are going to provide a selection of related research papers for each lecture on the course website.

EXAMS: We will have a final and a midterm. The exams will be designated as an open book/notes/... take-home to be submitted 24 hours after the release of questions (the following exam dates are to be interpreted as release dates).

Final:	Saturday, December 19, 13:30
Midterm:	Wednesday, October 28, 14:30

HOMEWORKS: There will be 4 homeworks. Homeworks may cover classic research papers, and include thought-provoking open-ended challenge questions.

PROJECT: We expect a small-scale research project. We encourage novelty, but you can also try to re-generate the results of an already published research paper. We will post a pool of ideas on the course website. You are encouraged to work in groups of up-to 3 students.

TOOLS: You may need an (micro)architectural simulator for the project. As an example simulator, SimpleScalar available in CSE Labs. However, you are not restricted to use SimpleScalar; the vast majority of simulators are open-source.

GRADING:		
	Final	20%
	Midterm	20%
	Homework ($\times 4$)	40%
	Project	20%

MECHANICS:

- Regarding academic integrity and scholastic dishonesty, according to the Office for Student Conduct and Academic Integrity (OSCAI), "Academic integrity is essential to a positive teaching and learning environment. All students enrolled in University courses are expected to complete coursework responsibilities with fairness and honesty. Failure to do so by seeking unfair advantage over others or misrepresenting someone elses work as your own, can result in disciplinary action. The University Student Conduct Code defines scholastic dishonesty as follows: Scholastic Dishonesty: submission of false records of academic achievement; cheating on assignments or examinations; plagiarizing; altering, forging, or misusing a University academic record; taking, acquiring, or using test materials without faculty permission; acting alone or in cooperation with another to falsify records or to obtain dishonestly grades, honors, awards, or professional endorsement." applies. **Independent of the scope (be it a homework assignment, exam, ...), any conduct leads to F as the immediate final grade.**
- The students are expected to attend all class meetings. Office hours are not designated to serve as make-up lectures.
- All assignments are due at the beginning of class, on the designated due date. Late assignments will receive a reduction of 20% for each day they are late, except for documented illnesses and family emergencies.
- Any question or concern about grading must be communicated to the TA or the instructor within one week after the return of the exam or assignment concerned.
- You can work in groups to discuss assignments, as long as the submission reflects your own work.
- UNITE students should submit all assignments according to the UNITE procedures.
- If the students fail to submit all of the homeworks, their final will not be graded.
- If the students fail to take the midterm, their final will not be graded.
- Any non-submitted or non-graded item will be processed with a grade of 0.
- Regarding incomplete grades, according to University Senate policy, "The I grade shall be assigned at the discretion of the instructor when, due to extraordinary circumstances, the student was prevented from completing the work of the course on time. The assignment of an I requires a written agreement between the instructor and student specifying the time and manner in which the student will complete the course requirements. In no event may any such written agreement allow a period of longer than one year to complete the course requirements." applies. An "I" will only be assigned if less than 15% of the course remains to be completed. In such a case, the "extraordinary circumstances" must be properly documented.
- Any student with disabilities to affect their ability to participate fully in class or to meet all course requirements is encouraged to notify the instructor so that appropriate accommodations can be timely arranged.

2 COURSE OUTLINE

- **Review**
  Impact of Technology on Computer System Design, Quantitative Analysis of Computer Systems, Pipelining Basics, Instruction Set Architecture, Memory Hierarchy
- **Instruction-Level Parallelism (ILP)**
- **Data-Level Parallelism (DLP)**
- **Thread-Level Parallelism (TLP)**
- **Warehouse-Scale Computers (WS)**

3 TENTATIVE TIMELINE

Week	Mon	Wed	Assignment	(Main) Reference
1	Labor Day	Review		H&P Ch. 1
2	Review	Review	HW1 out: Wed	H&P Ch. 2, App A/B/C
3	Review	ILP		H&P Ch. 2/3
4	ILP	ILP	HW1 due: Wed	H&P Ch. 3
5	ILP	ILP	HW2 out: Wed	H&P Ch. 3
6	ILP	ILP	**Project Proposal** due: Wed	H&P Ch. 3
7	ILP	ILP	HW2 due: Wed	H&P Ch. 3
8	DLP	DLP	**Midterm**: Wed HW3 out: Wed	H&P Ch. 4
9	DLP	DLP		H&P Ch. 4
10	DLP	DLP	HW3 due: Wed	H&P Ch. 4
11	TLP	TLP	**Project Progress Report** due: Wed	H&P Ch. 4/5
12	TLP	TLP	HW4 out: Wed	H&P Ch. 5
13	TLP	TLP		H&P Ch. 5
14	WS	WS	HW4 due: Wed	H&P Ch. 6
15	WS		**Project Final Report** due: Wed	H&P Ch. 6